REVIEW PAPER ON NEW TECHNOLOGY BASED NANOSCALE TRANSISTOR

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ABSTRACT

Owing to the fact that MOSFETs can be effortlessly assimilated into ICs, they have become the heart of the growing semiconductor industry. The need to procure low power dissipation, high operating speed and small size requires the scaling down of these devices. This fully serves the Moore's Law. But scaling down comes with its own drawbacks which can be substantiated as the Short Channel Effect. The working of the device deteriorates owing to SCE. In this paper, the problems of device downsizing as well as how the use of SED based devices prove to be a better solution to device downsizing has been presented. As such the study of Short Channel effects as well as the issues associated with a nanoMOSFET is provided. The study of the properties of several Quantum dot materials and how to choose the best material depending on the observation of clear Coulomb blockade is done. Specifically, a study of a graphene single electron transistor is reviewed. Also a theoretical explanation to a model designed to tune the movement of electrons with the help of a quantum wire has been presented.

KEYWORDS

MOSFET, SCE, Moore's Law, Nanoscale MOSFET, SED, SET, Coulomb Blockade, Graphene, quantum dots, quantum wire.

1. INTRODUCTION

The world goes round a transistor. The transistor is the bedrock of the processor. If the transistor was not invented our servers would have been three stories high. Without the transistor, probably the television would still run on vacuum tubes. Had it been the vacuum tubes a lot of tubes, bulbs and heat would have been required to accomplish the fundamental mathematical calculations. Indeed, when moths and other insects turned on the tubes and blowed them out, 'bug' was the term coined to represent the scenario. The size of the first transistor was as big as the palm of the hand. But today, forty-two years later a 45 nm Penryn chip has been invented that contains almost about 820 billion transistors [1].The little acclaimed transistor is analogous to an electronic lever. Just as the lever boosts the force required to get a work done, the transistor does the same. It allows for the regulation of a much larger current flowing through a channel by modulating the potency of a smaller current flowing through another channel. The transistors are highly rewarding owing to its small stature, less weight, low heat generation, low power dissipation and faster switching speeds [2].

They also find their utility in a wide range of applications but mainly as switches and amplifiers. One of the utility of a transistor is as an amplifier where a low power signal can be boosted [3]. The voltage of a signal can be surged by an amplifier from a microvolt range to a higher level of milli volt or Volt level. This happens because a small change in the base current results in a large change in the collector current.

When a voltage is enforced unto the base, the transistor turns ON and conducts current over the collector- emitter route. The absence of voltage results in the turning OFF of the transistor. The maximum bias voltage being 0.7 Volt. The switching on and off of the transistor can be done by varying the base current [4].

To curtail the size of the ICs in order to enhance the device functionalities, the transistor has been continuously scaled down. The actual size of the device has been reduced and there has been a rise in the number of transistors within a single IC and has been found to double after every 24 months as stated by Intel's Co- founder Gordon E. Moore [5]. In the year 1947, the BJT was invented. CMOS which has a compact size and is quite faster in operation came into being in order to supersede the BJT. Subsequent to the invention of the MOSFET in the 1970s, it has been the most prevalent semiconductor device.

This paper can be organised in various sections which are as follows. It is started off with the need for miniaturisation, the study of nanoscale MOSFETs and the various problems associated with them. Next a discussion on why Single electron transistor has gained popularity over MOSFETs is presented. A theoretical brief on the Single electron transistor is given followed by the different models of Single electron transistors. A brief explanation regarding the properties of quantum dot materials such as Silicon, Germanium and Silicon Germanium have been provided. This is followed by the study of Graphene Single electron transistor and how it is possible to tune the transport of electrons by means of a quantum wire. Finally, the discussion is wrapped up with a brief conclusion.

2. NEED FOR MINIATURISATION

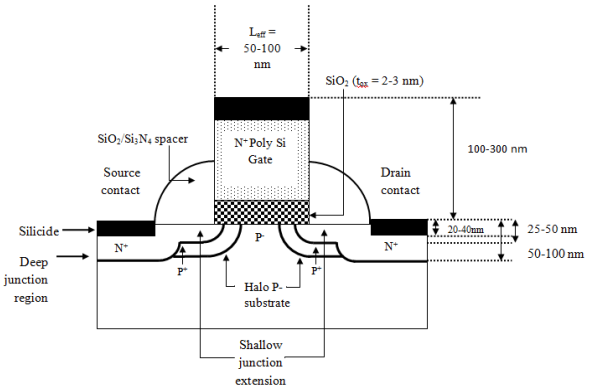
Device miniaturisation or downsizing is essential in order to achieve outstanding device performance at very low costs. It leads to the decrease in the cost per unit function and results in magnified device functioning. Compact dimensions of the circuits decrease the chip area on the whole. Therefore, more and more transistors can be placed in a single chip thereby reducing the manufacturing cost of the chips all together. Another usefulness of device downsizing is the decrease in the device power dissipation which is a boon to the mobile systems as it helps to extend battery life and helps in enhancing the reliability of high- performance systems. Since miniature chips expend lesser power, the energy utilized for each operation is also very less. As a result, the power delay product of the Chips is greatly diminished. On diminishing the MOSFET device dimensions there is a continuous decrease in the intrinsic switching time which is due to the fact that intrinsic delay is approximately equal to the channel length as well as the velocity of the carriers [6].

3. Nanoscale MOSFETs

Metal- oxide- semiconductor field effect transistor (MOSFET) is the substratum of the Integrated Circuit technology, the pillar of present- day computers and telecommunications. MOSFET has been employed tremendously in bulk silicon chips in the form of a dynamic component. The typical CMOS IC designs are executed by employing a pair of N- channel or P- channel MOSFETs. Hence, the penetration as well as its relevance in several fields for our daily needs requires to be barely reminded. Since the invention of the integrated circuit in the 1958 by J.S Kil by, the processing of semiconductor ICs have sustained an exponential growth [7]. This has come into being as a result of the continuous device downsizing or a persistent depletion in the minimum dimensions of the device [8-14]. To work towards attaining data processing as well as memory operations past the sub-micrometer dimensions and to a nanometer scale the decreasing of the size of the silicon MOSFET found integrated circuits have been extensively worked upon. For fabricating, an entire system on a single semiconductor chip it is important to draw attention towards MOSFET channel lengths of the order of 100 nm or below. So far MOSFETs having channel lengths of the order of several tens of nanometer are being produced in bulk whereas sub-10 nm MOSFET are being illustrated [15].

A comprehensive research has been going on for acquiring knowledge about the properties of nanostructures like Quantum Dots and two dimensional electron systems. In order to procure the requirement for excessive packing density and operating speed with ultra-low power dissipation; MOSFETs have been repeatedly scaled down. MOSFETs with gate lengths of the order of 10-100 nm exhibit complete performance. Even MOSFETs as small as 10 nm have been entrenched. Since these structures are acutely small their design, fabrication and understanding requires proper knowledge of device physics at both the sub micrometre and nanometre level. The simplified diagram of cross- section of a nano MOSFET is given in the figure below.

Figure 1: Diagram of a Cross-section of a nano MOSFET having a channel length of 50nm displaying typical dimensions and junction depths [6].



Crystal surface in the <100 orientation> is used while constructing N-channel MOSFETs on P-type Silicon wafers [16-21]. A retrograde type of channel doping profile is being utilised that grants for the utilisation of a high subsurface doping (5 × 10 17- 3 × 10 18 cm-3). This wards off the drain electric field from entering the source. A small surface doping of the order of 1×1017 cm-3 is done to retain the threshold voltage at a low level. The electron mobility is increased in the channel. This is done by reducing the impurity scattering in the channel [22-25]. Channel engineering is the term used to depict the adjusting of the channel doping profile [26-30]. The channel is interfaced by source/drain extensions having a small junction depth. However, in order to install a contact to the source/drain metal layers, rooted terminals are employed [31]. As Arsenic offers high solubility and a small diffusion coefficient, it is used as a dopant. To keep the resistance of the source/drain regions at a subordinate level refractory metal silicide such as Titanium Disilicide, Tantalum Disilicide, Platinum Silicide, Tungsten Silicide etc., developed [32]. The figure below shows a P and N- channel nanoMOSFET.

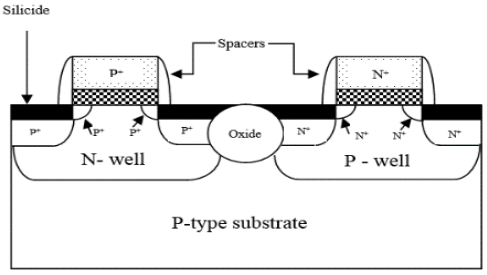


Figure 2: P and N – channel MOSFET [6].

Downsizing the MOSFET results in Short Channel Effects. As a result of the impact of the junction a considerable fragment of the channel region avoids gate control [33]. The deterioration of the subthreshold slope enhances the off state leakage current and this consequently increases the power dissipation. This phenomenon is known as the threshold voltage roll off. It is also observed that the off state current is enhanced as a result of the slashing of the source junction

barrier to minority carriers via the drain potential; this effect is known as the DIBL [34]. Retrograde or super steep retrograde profiles are utilised, in order to suppress the SCE [35]. In radically small devices a design that has gained recognition for the purpose of alleviating short channel effect is the DG MOSFET [36-38]. Apart from its ability to prevent short channel effect along with the possibility of downsizing to about ~10nm, the DG MOSFET also exhibits great transconductance and an approaching ideal threshold shift. One high- performance nanometer scale MOSFET is the DG MOSFET [39-41]. In order to overcome short channel effects; when a DG MOSFET adjusts itself and consists of a very thin silicon fin the resulting device is known as a FinFET [42,43].

Nano MOSFETs assure high operability, low power consumption and high packing density. The gate-source voltage needed to form a conductive inversion region between the source and the drain is termed as the threshold voltage and for a nano- MOSFET it is about 0.2-0.4 Volts. The transconductance must be maximal and it is given as:

$$g_m = \frac{\delta I_{DS}}{\delta V_{DS}} . \quad (1.1)$$

The channel conductance of a nano-MOSFET is defined as:

$$g_{DS} = \frac{\delta I_{DS}}{\delta V_{DS}} \quad (1.2)$$

under constant V_{GS}. g_{DS} should be maximum for operation in the linear area and for operation in the saturation area it must be minimum. NanoMOSFET exhibits a characteristic termedas subthreshold swing which demarcates the variation in the gate-source voltage essential to reduce the drain- source current by one decade. This subthreshold swing is given by

$$S = \ln 10 \frac{\delta V_{GS}}{\delta \ln I_{DS}} \quad (1.3)$$

As soon as I_{DS} drops to $1/10^{th}$ the worth of threshold voltage. In a nano MOSFET the S parameter inflicts a breaking point on the threshold voltage since the current has to be small enough to handle the off-state current.

4. PROBLEMS ASSOCIATED WITHNanoMOSFETs:

Few issues come up in the nano MOSFETs and they have been explained sequentially as to where they originate. The problems can be explained as below:

4.1 Channel

The problems that arise in the channel are categorised below and can be explained as given below:

4.1.1 Sub threshold leakage current

When VGS < Vth, a diffusion current flows between the drain and the source terminal. This diffusion current dictates the subthreshold leakage current. This subthreshold leakage current is also the weak inversion conduction current. As a switching device, it is contemplated to be a non-ideal characteristic of MOSFETs. The weak inversion conduction current can be represented as below [44]:

$$I_{subth} = \mu C_{dep} \left(\frac{W}{L}\right) V_T^2 \left(\exp\left(\frac{(V_{GS}-V_{th})}{\eta V_T}\right)\left(I - \exp\frac{-V_{DS}}{V_T}\right)\right) \quad (1.4)$$

Where $C_{dep}= \sqrt{\frac{\varepsilon_{Si} q N_{sub}}{4\varphi_E}}$ indicates the capacitance of the depletion region beneath the gate area, VT represents the thermal voltage and is given by $\frac{kT}{q}$ and lastly n denotes the sub threshold parameter which can be given as $1+C_{dep}/C_{ox}$.The subthreshold slope can be generated from the above equation. With an increasing VGS and decreasing V_{th}, I_{subth} increases exponentially. Calculating the partial derivative of $\log_{10} I_{subth}$ with respect to V_{GS} results in a constant slope labelled sub-threshold slope and this is given as:

$$SS=\frac{\delta log_{10} I_{subth}}{\delta V_{GS}} = \frac{I}{\ln 10\, I_{subth}} . \frac{\delta I_{subth}}{\delta V_{GS}} \qquad (1.5)$$

It can be concluded here that with decreasing voltage, the transistor turns off unanticipated. For the transistor to turn off adequately, S must be designed such that it is as small as possible. At room temperature, S is always greater than 2.3VT (~ 60mV/dec). This indicates how strongly the gate contact can command the channel surface potential. Utilising a thinner gate oxide thickness S can be made petite. This leads to a larger Cox. Lowering the substrate doping concentration also results in a smaller S.

4.1.2 Threshold Voltage variation

The device speed and sub threshold leakage current is analogous to the threshold voltage (Vth) change. As a result, it needs to be curtailed. Chiefly, this can be justified in terms of two parameters. One is Vth roll off and the other is DIBL (drain induced barrier lowering). In an identical synonymous wafer, the transistors with a dissimilar channel length (L) results in a varied Vth. Owing to a condensed channel length, the threshold voltage dwindles thus exhibiting Vth roll off. In addition to reducing Vth as a result of growing drain voltage describes DIBL. Vth roll off and DIBL springs up from the descending potential barrier between the drain and the source. This happens because of the rise in the charge – sharing effects amidst the channel and the source/drain depletion regions. Charge – sharing effects causes a transistor to utilize less gate voltage in order to deplete the substrate that lies below the gate dielectric and reduces Vth [44 - 46]. Alongside an added rise in the drain voltage the depletion region about the drain goes on to lengthen to the source depletion region and eventually fuse together ahead of junction breakdown. On the other hand, the drain current escalates as a result of the subsistence of a parasitic current route. This is known as punch- through. A rise in the comprehensive substrate doping will help in prohibiting punch through. Yet a greater doping will also lead to an upsurge in the sub threshold swing. Hence decreasing the leakage current is not feasible [47, 45, 48]. These entire phenomena are accredited as Short Channel Effects. SCEs influence the rise in power consumption and hence to alleviate SCEs nano MOSFETs came into being.

4.1.3 Carrier mobility degradation

The electric field under the MOSFET keeps on growing. This occurs as a result of the depletion in the rate of voltage scaling and geometrical scaling is maintained at the same historical rate. At a low field of the order of less than 103 V/cm, the drift velocity of the carriers is proportional to the longitudinal electric field over the channel. At room temperature, the rising longitudinal field in Silicon leads to a reduction in the growing rate of the carrier's velocity. Eventually when the electric field will raise above 3×104 V/cm for electrons and 105 V/cm for holes, the carriers will reach their maximum velocity; given by Vsat ~107 cm/sec. This phenomenon where the degradation of carrier mobility occurs is known as velocity saturation and occurs due to a number of reasons such as phonon absorption, dispersion, emission and energy band parabolicity [49, 50].One higher electric field fosters between the gate and the channel as a result of encroached scaling of the gate oxide thickness for constant voltage supply leading to a confinement of the charge carriers to a constricted region beneath the oxide- Silicon interface inducing greater scattering of carriers and consequently reduced mobility.

4.1.4 Hot Carrier Effects

The high electric fields inside equipment cause HCEs as a result of which issues like shift in the threshold voltage and deterioration in the transconductance are caused. The carriers acquire high Kinetic energy consequently due to a rise in the scattering rate of the steep electric fields. This rise in the scattering rates of the large electric fields occurs due to the saturation of the typical speed of the carriers in the channel. As soon as the energy acquired by these hot carriers is enough to surpass the barrier they may relocate to undesirable regions like the transistor gate, transistor substrate and gate dielectric. By means of "Impact Ionisation", the immensely accelerated hot carriers present close to the drain have the ability to create fresh electron-hole pairs as a result of striking with the Silicon atoms. Due to Impact Ionisation a rise in the substrate current occurs which implies that carriers are introduced in the gate dielectric. Therefore, charges are confined in the gate oxide. This leads to a threshold voltage swing and the device becomes volatile and may malfunction [49,51].

4.1.5 Direct source to drain tunnelling

When the transistor channel length (or the barrier width) separating the source and drain turns out to be so small that the electrons can tunnel through the barrier without the application of any added gate bias externally, the use of MOSFET as a switch is not possible now. In distinction to the eminent Shannon- von- Neumann Landauer (SNL) expression, taking into account only the transport of electrons across the barrier but the direct tunnelling of electrons, the minimum energy barrier in order to set apart two different states of electrons at room temperature is given by ESNL= kBT(ln2) = 0.017eV. Here kB is the Boltzmann's constant and T represents the temperature. Hence, the minimum energy imperious to process a bit is Ebit>ESNL = 0.017eV. With respect to quantum mechanics, the least possible channel length apt to refrain Ebit, in order not to let tunnelling occur is about 5nm. It is possible to obtain a petite channel length by augmenting the Ebit. Consequently, a trade-off must be made with the burgeoning of total power dissipation. Thus, to meet this need, requirement of improved cooling techniques become a fussy issue [52,53].

4.2 Gate

The problems that arise at the gate terminal are categorised and explained as under:

4.2.1 Direct Tunneling gate leakage

Amidst the rapid scaling of MOSFET going on, the gate oxide thickness has been subsequently cut down to retain the gate controllability across the channel. Still when the thickness of the gate oxide is lowered below 2nm, as a result of quantum mechanical tunnelling the direct tunnelling gate leakage rises exponentially. As a result, not only this condition leads to a rise in the standby power dissipation but also curbs the proper functioning of the device [54].

4.2.2 Gate Depletion

Because of better thermal stability to higher processing temperature, Aluminium was replaced by Poly-Si and since then it has been extensively used. Further, the use of Poly-Si has limited the overall number of processing steps by way of self-aligned processing. Here, for the creation of source and drain junction, the gate is used as a hard mask at the time of ion implantation. As a result of this technique a tighter overlap is granted over the gate and source/ drain regions leading to lower parasitic capacitance. Additionally, the work function of Poly-Si can be easily tuned by regulating the doping concentration [55]. In spite of heavy doping of the Poly-Si gatehas an assured resistance and that grants a considerable RC time delay. Further inadequate doping of the Poly-Si also results in an effect known as the Poly-depletion effect where the region in the poly Si gate electrode adjacent to the Poly-Si /SiO2 interface becomes depleted with carriers. Therefore, Poly-Si is not a satisfactory material for future gate electrodes and calls for the requirement of new materials.

4.3 Drain/Source

The problems that crop up at the drain- to- source region are categorised and explained as under:

4.3.1 Parasitic resistance

In the process of further scaling down of the device, there is an authority of parasitic resistance on the on-current and it tends to rise somewhat greatly. For that reason, there must be an appropriate regulation of the parasitic resistance to obtain better device functioning. The total parasitic resistance can be branched into four parts like overlap resistance, extension resistance, deep resistance and Silicide diffusion contact resistance [56]. The total parasitic resistance resolves the voltage drop between the channel and source/drain contacts [56]. It is desirable to have a superficial source /drain junction depth in order to hold down the short channel effects adequately. But shallower junction also calls for the increase in the sheet resistance as a result of which the doping must also be raised likewise in order to keep the sheet resistance constant.

4.3.2 Parasitic Capacitance

The reason behind the revved-up CMOS circuit design is the lower capacitance and higher drive current; owing to the conventional CMOS inverter delay model which is given by CG VDD/ID. In this manner, with geometric scaling, we can acquire satisfactory device performance as the gate capacitance comprises of the intrinsic gate capacitance as well as the parasitic gate capacitance. The gate capacitance declines in proportion with the gate length abatement in micro MOSFET. But, when the MOSFET breaks into the nanometre regime, due to the rise in the parasitic capacitance there is no subsequent fall in the gate capacitance proportionately with the gate length minimization. Accordingly, to keep up the performance betterment from scaling, it is important to keep a track of parasitic capacitance reduction techniques [57].

4.4 Substrate

The problems that crop up at the substrate are classified and explained below. The substrate leakage current mostly comprises of the impact ionisation current, reverse biased junction leakage current and GIDL current.

4.4.1 Reverse Bias Junction Leakage Current:

The current flowing between the Source-drain and the substrate over the reverse biased pn-junction diode in the off-state MOSFET is called the reverse biased junction leakage current (I_{rev}). I_{rev} relies upon the junction area and the doping concentration. Hence, various devices in order to reduce BTBT current are being designed.

4.4.2 GIDL:

GIDL current is one of the chief off-state leakage current components and is sometimes also termed as the surface BTBT current. When the supply voltage biases the drain of an n- MOSFET and the gate is either biased by a zero voltage or a negative voltage, a depletion region shapes up beneath the gate and drain overlap region. Due to the reverse bias between channel and the drain if a high electric field is induced in the narrower depletion region then a convincing amountof surface BTBT current flows/passes over the drain to the substrate junction. Materials possessing smaller band gaps increase the GIDL current.

5. THE SINGLE ELECTRON TRANSISTOR

The Single electron transistor or SET is the ultimate basic three-terminal single electron device [58-60]. The simplified diagram of a SET is given below in the figure. The configuration of a

SET is similar to that of a MOSFET. SET can be seen as a quantum device that operates on the principle of single electron tunnelling through the tunnel junction [61]. It has a conducting island that is linked to the source and the drain terminals. While being capacitively connected to one or more gate terminal. The gate terminal is responsible for the transmission of individual electrons between the source and the drain terminals. The tunnel junction is considered to be a small insulating barrier that lies between two electrodes which are conducting. The Single electron charging effect or the Coulomb Blockade is an important phenomenon taking place in the SET, by means of which an exact regulation on the movement of the number of electrons is made. Further as a result of the decrease in the number of electrons in a switching transition, there is a significant decrease in the circuit power consumption [62].

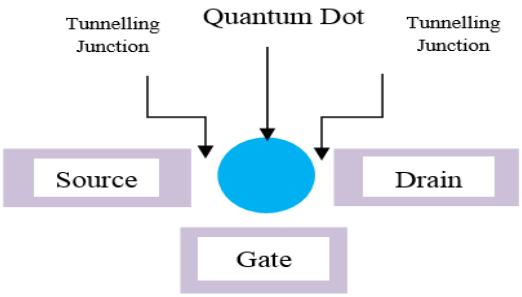


Figure 3: Schematic Diagram of a SET [63]

6. DIFFERENT MODELS OF SINGLE ELECTRON TRANSISTOR

Single Electron Transistors exhibit fresh performance characteristics that makes them favourable suitors for fabrication of CMOS VLSI and hybrid CMOS/SET based ICs. SETs are also utilised in applications concerning charge sensing and accurate measurement applications in metrology. In Single Electronics the Orthodox Theory is the bedrock of the few models of Single electron device. A good deal of quantum mechanics is often overlooked in nearly all the models that are established upon the Orthodox Theory. As a result, these models are assumed to be semi-classical.

According to some models, the action of tunnelling where the electrostatic energy is responsible for the transport of electrons through the barrier is statistical in nature. The frequency at which tunnelling occurs relies on the emerging adjustments in the system's free energy. As soon as the tunnelling rates of all the tunnelling junctions are investigated, Monte Carlo simulation method [64] is employed to deduce the real tunnelling events that occur and hence the simulation of random dynamics of single electron systems is possible. Monte Carlo simulation technique is enacted in several programs like SIMON [65], MOSES [66], KOSEC [67] and SECS [68]. The tunnelling dynamics required to examine circuit functioning is modelled by the Monte Carlo simulation method. It helps in explaining the underlying principles of the system.

The Master Equation modelling method is employed in the simulation of Single electron circuits and is established on the Orthodox Theory. The Master equation on the contrary is anillustration of the fundamental Markov process [68] of the tunnelling of electrons from one island to another. As a result, the circuit moves into dissimilar states. Here, one requires the set of all the possible states that the circuit occupies. The states are described by the distribution of charges and the external voltage supplies. However, to crack the Master Equation, one must consider only a specific number of states.

There are several models. They are described as under:

6.1 The Macro Model

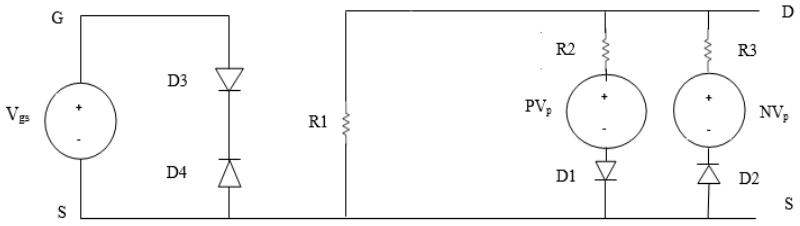
Subjected to conventional CMOS designing of circuits: the device modelling and circuit simulation for the designing of SET based circuits would be a prospective step. While compact

simulators like SPICE are being employed for the simulation of the attributes of the given topology of the circuits in conventional circuits. Here, two assumptions are essentially utilised to frame the model.

First, when the specification of the secluded transistor is resolved from the device simulator or any other modelling equipment, it can be employed in the overall circuit. At the same time, when the device simulator describes the model attributes, the device I-V characteristics behave as a function of the device width.

Second, the adjacent transistors have an effect on the I-V characteristics of the device as a result of change in the terminal voltage of those transistors. The intercommunication between the neighbouring devices are normally overlooked. However, with SET based circuits the second assumption may not hold true. This is because meanwhile when a number of SETs are connected, the charge states of the adjacent islands of the distinct SETs may influence the charge states of the Coulomb Islands of the SET. Still at identical bias condition, the terminal currents of the circuit SET may differ from that of the secluded SET. For the employment of complete simulation techniques to single – electron circuits. Compact modelling is necessary for the depiction of the characteristics of the secluded SET in preference over the characteristics acquired as a result of the Monte Carlo technique. Wu established a macro modelling to SET that is completely congruent.

Figure 4: Figure: Macro model proposed by Yu [69]



D2 and D2 are facing D3 and V3 so as to possess sufficient current flow in both the positive and negative drain to source voltage. The charging energy systematically varies as a function of the gate voltage. The charging energy is comprehended in R1, R2 and R3 which utilizes the cosine of the gate voltage. In the model developed by Wu, with the rise in the gate- source voltage 'V_g' the I_d rises and this is displayed in the $I_{ds} – V_{gs}$ characteristics. This occurs as a result of the passing of the leakage current between the gate and the source terminals. Likewise, the equation given by Yu's model fails to portray the exponential behaviour of the Coulomb Blockade meticulously in its output characteristics. Hence, Wu and Lin developed a revised compact macro model for SET. It can be seen in the figure below.

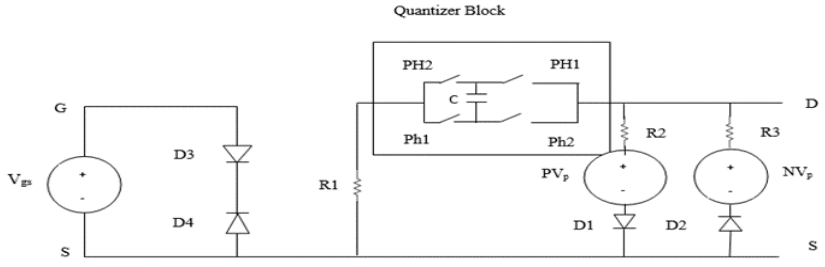


Figure 5: SET model developed by Macro- modelling consisting of a quantizer block [69].

A bigger resistance is employed in place of two optimal diodes D2 and D3 placed confronting each other in order to prevent the flow of all the probable currents starting with the gate and entering the source, induced by the use of gate-to- source voltage (Vgs). In this model, two sections consisting of an integration of resistors, diodes and voltage sources are incorporated. R1 behaves as the primary resistance in the region of Coulomb Blockade where R2 and R3 represent the resistances in the non- Coulomb Blockade region while the drain and source are being appended in the model in both the positive as well as negative course. The division between the Coulomb Blockade and the non-Coulomb blockade region is determined by the source voltage Vp attached in each section of R2 and R3.

6.2 Analytical Model

For a SET, several analytical models have been established. One of the models established by Wasshuber was based on the notion of free energies of the tunnelling junctions. But in the model developed by Wasshuber, tunnelling of electrons over a single tunnelling junction is examined at a time. However, this does not reveal the genuine condition of operation of SET, consisting of two tunnelling junctions and a supplementary capacitor attached to an island at the centre that is conductive.

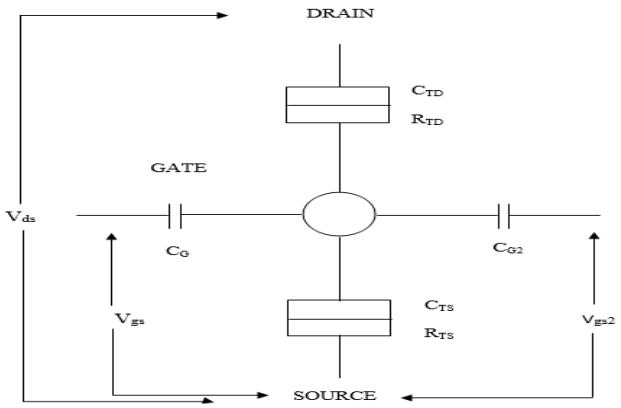


Figure 6: SET circuit exhibiting the subsistence of overall resistance and capacitance [69].

The assumptions that go into extracting the analytical model for SET are as under:
First, the entire source and the drain terminals of a SET is linked to capacitors whose capacitance is much bigger than the complete capacitance of the island of the SET or else the biasing of the source- drain terminals by a constant voltage source. This model promises that only the adjacent circuit elements will influence the output characteristics of the SET by means of node voltages on the SET terminals. Second, the resistance of the source and the drain is believed to be identical. However, this assumption lays a minor constraint on the SET configuration. But it minimises the calculation job significantly and also provides a straightforward yet brief ultimate formula.
Two of the compact numbers of electrons in the island of the SET are considered for each value of the gate voltage. This steers the double-junction analytical model of SET which is built on the grounds of the 'Orthodox Theory' and also the steady- state Master equation method. On the grounds of the above equations the Master equation can be deliberated precisely.

6.3 MIB Model

The MIB model has been titled on the names of its creators. They are Mahapatra, Ionescu and Banerjee. The MIB model has been established on the Master equation method. This model is appropriate for the design of digital and analog circuits since this model is restricted to |VDS |< 3e/C. besides, this model confers and easy and streamlined technique to obtain the parameters of

the model to obtain a familiar asymmetric device that is necessary for the designing of SET based circuits [70].

The following assumptions are the foundation of the MIB model.

First, the Orthodox Theory of tunnelling of single electrons are followed.
Second, the linking capacitances related to the gate, source and drain terminals are considerably bigger than the capacitance of the device assuring that the overall capacitance of the island with reference to ground is equivalent to the addition of all the capacitances of the device. As a result, there is no synergy amidst the interconnected SETs. It is given as:

$$C_{\sum}=C_{TS}+C_{TD}+C_G+C_{G2} \quad (1.6)$$

The second assumption possibly requires a little more explanation. In order to clear out the confusion, it is necessary to understand the distinction between SED and SET. SET is a certain form of SED whereas SED is an arbitrary package of various conductive islands which are joined to one another and outside by means of tunnel junctions or capacitances. Practically, the capacitance of the interconnects are bigger than the device capacitance of the SET and hence the second assumption holds true.

The MIB model has been established on the basis of three significant steps and they are: (a) determining the island potential, (b) swinging the drain current window and (c) determining the drain current.

6.3.1 Determining the island potential

With the employment of definite external voltages such as VGS, VGS2 and VDS ahead of electron tunnelling and tunnel junctions portraying the capacitances, the island potential can be demonstrated as:

$$V_{island} = \frac{C_{TD}}{C_{\sum}}V_{DS} + \frac{C_G}{C_{\sum}}V_{GS} + \frac{C_{G2}}{C_{\sum}}V_{GS2} - \frac{\varsigma_e}{C_{\sum}} \quad (1.7)$$

Where ς is a real number that gives the background charge. The electron tunnelling across a barrier or tunnel junction can be administered by the overall Thevenin capacitance $C\sum$ belonging to all the related islands with reference to ground. Hence the Thevenin capacitance of any SET relies on its self-device parameters. Besides it also relies on the parameters and alignment of the different SETs. This difficulty can be resolved if the second assumption remains valid.

6.3.2 Swinging of the drain current window

The drain current changes proportionately as a function of Visland accompanied by a regularity of 2α. The drain current equation in the MIB model has been established supposing the period : $\frac{V_{DS}}{2} \leq V_{island} \leq 2\alpha + \frac{V_{DS}}{2}$. An integral multiple of 2α is used to swing the values of the V_{island} into the drain current window and the identical model can be utilised to compute the drain current. This swing in the drain current can be accomplished as shown below:

If $\lambda V_{island} > \frac{2\alpha + \lambda V_{DS}}{2}$

$V_{island} \leftarrow V_{island} - 2\lambda\alpha \left(1+\left[\frac{|V_{island}-2\alpha-\frac{\lambda V_{DS}}{2}|}{2\alpha}\right]\right)$

If $\lambda V_{island} < \frac{\lambda V_{DS}}{2}$.

$V_{island} V_{island} + 2\lambda\alpha \left(1+\left[\frac{|V_{island}|-\frac{V_{DS}}{2}|}{2\alpha}\right]\right)$

6.3.3 Determining the Drain current

For a particular bias, for the computation of drain current for the specified condition of $|VDS| < \frac{3e}{C_{\sum}}$, two possible number of electrons supposed are 0 and 1. This means that the number of electrons

that reside on the island can be 0 and 1. In this model, by resolving the steady state Master equation, the drain current can be determined. By resolving the Master equation for the state transitions '0 to 1', '1 to 2', '-1 to 0', and substituting the tunnelling rates with tunnelling currents and applying Gibbs free energy, the drain current expression from the MIB model is compound. Although by implementing certain smart presumptions the complications of the model can be reduced without getting rid of the remarkable accuracy. It was also stated earlier that the tunnelling of electrons at every tunnel junction takes place in two directions. Since the tunnelling rate taking place in the direction of higher potential is substantially larger than the one taking place at the lower potential it leads to a considerably clearer model outline of the MIB model. This can be shown as under:

$$I_D = \lambda \frac{I_{TS}(0)I_{TD}(1) + I_{TS}(0)I_{TS}(1) + I_{TD}(1)I_{TD}(0)}{I_{TS}(0) + I_{TD}(1) + \frac{I_{TS}(0)I_{TS}(1)}{I_{TD}(2)} + \frac{I_{TD}(1)I_{TD}(0)}{I_{TS}(-1)}} \quad (1.8)$$

Assuming only '0 to 1' transition of states, the equation of MIB model can be simplified and written as follows:

$$I_D = \lambda \frac{I_{TS}(0)I_{TD}(1)}{I_{TS}(0) + I_{TD}(1)} \quad (1.9)$$

This equation portrays the fact that the device currents is only as half of the harmonic average of the drain tunnelling current as well as the source tunnelling current [71].

7. DIFFERENT MATERIALS FOR QUANTUM DOTS

With the ongoing trend of the semiconductor industry the main question is how small can we go? The explanation is as small as a quantum dot. A quantum dot is a particle that is of the size of about one billionth of a meter or in other words about 1 nanometer in size. Quantum Dots are generally made up of materials like Silicon, Germanium, Silicon Germanium, Graphene and several others. A quantum dot is a mesoscopic system that is almost smaller than a 100 nm in size. Here the electrostatic energy also known as the coulomb energy can be modified as a result of the withdrawal or inclusion of individual electrons. This energy is greater than the thermal energy of the system and can govern the movement of electrons in and out of the quantum dot. Basically a quantum dot is a conducting island that consists of an adjustable sum of electrons that populate discrete orbitals. Due to the quantum size effects, semiconductor QDs displays outstanding optical and electrical properties. One such property is the visible photo luminescence in porous Si which has gained quite some popularity over the last decade. When the size of the semiconductor materials is diminished beyond the Bohr radius (a_β), degenerate energy bands breach into discrete levels with enlarged bandgaps as a result of which the quantum dots become further identical to molecules than bulk materials. Semiconductor materials often consist of electronically active surface as it embodies unsaturated surface bonds or suspended bonds. Because of extensive surface- to- volume ratio, the personification of surfaces is especially important. To confirm the satisfactory confinement of electrons inside the QD, these unsaturated surface bonds must be disposed of and this is done by surface passivation. Since the past 10 decades, there has been a comprehensive investigation regarding the study of the effect of quantum confinement on the physical properties of semiconductor materials. For an outstanding SET's operation at room temperature requires two chief facts must be effectuated: one is to shun the thermal perturbation, the energy level disunion within QDs should be larger than the thermal energy ($\Delta E > k_B T$) and the other is to diminish the cotunneling noise, by making the charging energy greater than thermal energy and tunnelling rate ($U > k_B T$ and $U >> \Gamma$). Taking these points into consideration, germanium QDs would be more fascinating for the application in single-electron (or single-hole) device because lower-energy band gap and smaller carrier's effective mass would aid in stronger carrier confinements and larger energy level separations set side by

side to Si QDs at the same size. The effective mass of electrons in a spherical QD were approximated by $m^* = 3/(1/m_l+2/m_\tau)$, where $m_l$and $m_\tau$represents the longitudinal and transverse effective mass of bulk material, suitably. In nanometre scale materials, the conception of effective mass substantiates to work better and so it is feasible to await that the criterion inflicted on the QD size for room temperature SETs is less rigid in the case of Germanium.Due to the fact being the lattice constant of germanium is 4.2% larger than that of silicon, the Vegard's rule can be utilised to approximate the lattice constant of a bulk SiGe alloy [72]. The Vegard's rule employs a linear interpolation of the parameters of the end-point elements of Si and Ge. Bands in SiGe are firmly influenced by strain and the heavy hole/ light hole splitting persuaded by strain results in the branching of the valence band. This strain induced arrangement of the bands largely influences the mobility of electrons in strained Si.

What is most surprising is the fact that the discovery of Ruess, Vogt, and Hofmann, went hugely unseen and there were only theoretical publications during the following years. Mouras et al, was the personality responsible for framing the term "graphene", in 1987. Graphene Quantum Dots (GQDs) can be defined as small graphene particles that are characterized by restricted transport of electrons in all three spatial dimensions. Graphene can also be seen as a zero bandgap semiconductor that possess an infinite exciton Bohr diameter [73]. As a result of which, confinement can be noticed in any fragment, but GQDs have dimensions below 20nm. In theory, Graphene is an excellent atomic monolayer with infinite 2D expansion [74].At room temperature, the electron mobility in graphene is found to be almost as high as 15000 cm2 V-1 s-1 with limited dependence on temperature and zero effective mass for the charge carriers [73]. This low temperature dependence signifies that the motion of electrons is obstructed by defect scattering only and not by phonon scattering as is the case in most materials. Hence, Graphene has a resistivity of 10-6 Ω cm and this makes it the material with lowest resistivity at room temperature. Graphene exhibits special electronic properties that are dissimilar to other materials. Following are the causes behind this. First, the electron spectrum of Graphene is illustrated by a Dirac- like equation instead of a Schrodinger equation. Second, in graphene the electron waves circulate in layers which is a single atom thick modelling them to be more accessible to several scanning probes. Third, the electrons in graphene can traverse submicron distancewithout scattering. Because of the massless character of carriers in graphene and subdued backscattering, the quantum effects in graphene are resilient and can even strive at room temperatures. Since graphene has many unique properties under its hold, graphene may overtake Silicon as the base electronic material and delve into the "beyond the age of Silicon". Therefore, we study about Graphene Single electron transistors.

8. GRAPHENE SINGLE ELECTRON TRANSISTOR

To be effortless, we can define graphene to be a thin layer of pure carbon. Graphene is characterised as a single, firmly packed layer of carbon atoms where the atoms are bonded together in a hexagonal, honeycomb lattice. It is an allotrope of carbon. It forms a structure of a plane of sp2 bonded atoms having a molecule bond length of about 0.142 nanometres. Graphite is created by mounting layers of graphene on top of each other keeping an interplanar spacing of 0.335 nanometres in between. It is the thinnest and the lightest compound known to man standing at one atom thick. It is also the strongest compound known and is believed to be 100-300 times stronger than steel and has a tensile stiffness of 150,000,000 psi. It is believed to be the best conductor of heat and electricity at room temperature. Graphene also displays some excellent optical properties. Graphene exhibits spectacular band structure properties. Surface contamination does not affect the electron transportability and it is found out to be exceptionally high even at room temperature. When set side by side to utterly high quality semiconductor materials like Silicon and GaAs; the study of electronic transport in graphene is still in its inception.

SETs are constructed of a small sub-micron sized island, which is coupled to source and drain terminals [75]. There is the theoretical study of bound states in narrow graphene ribbons for a

given number of boundary conditions [76, 77]. In an experimental set up it has been displayed that a graphene island with a size smaller than 100 nm is connected through two graphene constrictions to wide graphene contact regions [78]. The strong influence of inhomogeneity and the coulomb blockade effect in constrictions, raises the question, that in a similar structure whether it is in any mannerfeasible to detect a clear Coulomb blockade effect derived from charging the graphene island. Additionally, the study of quantum states and quantum confinement have been kick-started due to the viewing of the Coulomb blockade effect in graphene. If at an extremely low source to drain voltage i.e., $V_{SD} << k_BT$, the conductance is to be determined, the transport of electrons is realizable in an energy window specified by the temperature of size k_BT [75].

The initialmarks for the significance of size quantization in these structures, and the likelihood of the analysis of excited state spectra [79], are the resonances running in parallel to the Coulomb blockade diamond boundaries and it is evident that the physicists exercise the term “quantum dot” rather than “single-electron transistor”, once the size quantization becomes significant. Identification of spin states and the experimental deduction of the *g*-factor of graphene [80] are upcoming difficulties in this field of research. One more open question is associated with the spin- and valley degeneracy in bulk graphene. In carbon nanotubes, shell filling is noted and there is a viewing of a four-fold filling periodicity compatible to the two-fold spin and the two-fold valley degeneracy. However, no such shell filling has been noted in graphene, until now. Anequivalent aspect is the traversal from electron- to hole-confinement in graphene, where initial experiments have been announced [78], yet the nature of the data is still left far beyond the comparable measurements in carbon nanotubes.

For all these experiments and related future progress in the field, enhancements in material quality will be vital, as they would lessen the impact of disorder-induced effects that are restricting experiments today and only then it will be viable to address even more leading concepts of information processing schemes with spin-qubitsin graphene quantum dots that have been theoretically recommended [81]. The presentation of an integrated graphene charge-readout [82] as it is familiar from the well- accepted Ga[Al]As systems [83], is one first experiment in this direction. Recent experiments have revealed that it is feasible to fabricate and inspect systems with current material quality and technology [84,85]. In the coming times, such systems may permit scientists to detect effects like the spin-blockade, and to execute coherent spin-manipulation approach, again known from Ga[Al]As studied so far [86,87]. However, there has been aforecast of graphene presenting crucialbenefitsmatched to this well-accepted material system: quantum de-coherence because of nuclear spins and spin orbit interaction restrict the performance of GaAs spin-qubits today. However, it is believed to be notably reduced in graphene, since the density of nuclear spins is particularly small and spin-orbit interaction is apparently weak.

9. TUNING OF ELECTRON TRANSPORT IN A QUANTUM DOT USING A QUANTUM WIRE

The electron transport properties in a quantum wire connected to two metallic bodies are investigated. a simple tight-binding model is utilised to illustrate the system and the connecting of the wire to the source and the drain electrodes is handled by means of Newns-Anderson chemisorption theory. In this present model, the site energies of the wire are expressed as: $\varepsilon_i = W\cos(i\lambda^{\nu}\pi)$ where W, λ, ν are three positive numbers. For ν =0, by adjusting the strength of the potential W, an easy regulation over the threshold bias voltage of conductionof electrons over the bridge is gained. Whereas for ν≠0, the wire becomes aperiodic and interestingly it is observed that for some particular values of ν, there is a display of a metal insulator transition which provides a significant feature in this particular study. Owing to reduced system dimensionality and lateral quantum confinement, quantum transport in low dimensional systems such as quantum

wires, quantum wells and quantum dots imparts various novel characteristics. What makes them indeedspecial is their geometrical sensitivity that offers the likelihood of exploring quantum transport in a very adjustable environment. There are variousattributes that command the transport of electronsover bridge systems and all these factors have to be taken into consideration properly to specify such transport. The model and method for determining the transmission probability (T), conductance (g) and current (I) by means of a quantum wire coupled to two metallic electrodes that are one dimensional is carried out by means of Green's function technique. The figure is shown below. In case of a small bias voltage and temperature, the conductance (g) of the wire is calculated by using the Landauer formula for conductance [88,89]. It is given as:

$$g = \frac{2e^2}{h}\ T \tag{2.0}$$

where T is the transmission probability and can be given as [88,89]:

$$T = \mathrm{Tr}\ [\Gamma_S G_w^r\ \Gamma_D\ G_w^a] \tag{2.1}$$

Here G_w^r and G_w^a resemble the leading Green's function of the wire. Γ_S andΓ_D represent the linking of the wire to the source and the drain terminals.

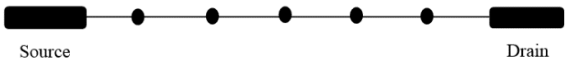


Figure 7: Simplified diagram of a quantum wire coupled to the source and the drain terminals with the black dots representing the on-site atoms in the wire.

The Green's function can be given as:

$$G_w\ = (E - H_w - \sum_S - \sum_D) \tag{2.2}$$

Here E represents the energy of inserting an electron and H_w resembles the wire's Hamiltonian. This Hamiltonian can be expressed as:

$$H_w = \sum_i \epsilon_i C_i^\dagger C_i + \sum_{<ij>} t\left(C_i^\dagger C_j + C_j^\dagger C_i\right) \tag{2.3}$$

In the above equation, $C_i^\dagger C_i$exhibits the formation operator of an electron on site;i ,$\epsilon_i$are the on-site energies and t representing the adjacent- neighbour hopping power. In a current research, the relation between the on-site potentials are expressed as:

$$\epsilon_i = W cos(i\lambda^\nu \pi) \tag{2.4}$$

Here W is the strength of the potential whereas λ and ν are the positive numbered parameters that exemplify the question of tight-binding. The wire turns periodic (ν=0) and aperiodic (ν≠0) built upon the value of ν. The Newns – Anderson model allows for the characterisation of the conductance concerning the wire attributes which is multiplied by the effective densities of the states that include coupling and also permits to carry out the research on conductance as a function of the attributes of the wire's electronic structure that connects the electrodes. The current that flows along the wire can also be considered as a single electron scattering process amidst two banks of charge carriers,

10. CONCLUSION

The different models for SET have been analysed. The MIB model has been validated by simulating it with the MC based simulator SIMON. Background charges are generally found near the SET grain or dot. They usually emanate from the ionised impurities or charges that are trapped. The fact that when the background charge is an integer times of the fundamental

electronic charge 'e' there are no variations in the output characteristics of the SET. But, when the background charge is a fractional number, the output characteristics are swinged by a value of $e\varsigma_{eff} / C_G$. It was also established that the Monte Carlo based simulators are extensively time expending whenever the simulation demands a high temperature operability or a SET biased by a current or whenever a SET based circuits incorporates a resistance. The factors like capacitance, mobility of electrons, its structure specifically crystalline, simplicity of fabrication and simplicity of the growing process of the oxide layers determine the material that will be utilised in the making of a SET. The island size must be really small of the order of nanoscale in order to operate at room temperature. Graphene has a conductivity that is better than Silicon and a lower resistivity which makes it an acceptable material for making the island of the SET since it allows for better electrical conductivity. By now a bi-layer graphene is being examined deliberately since this material allows for the tuning of the band gap by gates that are electrostatic. Besides a fascinating aspect of Graphene being the next basic electronic material after Silicon is the possibility of creating devices with superconducting [90] or ferromagnetic [91] contacts. Green's function has been utilised in order to study the electron transport characteristics in a quantum wire. Here for distinct values of ν related to individual regimes. By adjusting W, the variation in the band gap can be done in the conductance spectrum which is accountable for the persistent flow of current for a range of bias voltages. Metal-insulator transition is observable in the system. As a result, one can regulate the Fermi energy to an acceptable energy zone within the spectrum that allows for the regulation of the transmission characteristics in the quantum wire that also can be employed in developing a switching device.

ACKNOWLEDGEMENTS

I am using this opportunity to express my gratitude to everyone who supported me throughout the course of this M. Tech project. I am thankful to my professors for their aspiring direction, invaluably constructive criticism and friendly advice during the project work. I express my sincere thanks and heartfelt gratitude to my parents and friends for their never ending love, support and encouragement which have enabled me to overcome all the hardships all throughout.

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