DESIGN OF DIFFERENT DIGITAL CIRCUITS USING SINGLE ELECTRON DEVICES

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ABSTRACT

Single Electron transistor (SET) is foreseen as an excellently growing technology. The aim of this paper is to present in short the fundamentals of SET as well as to realize its application in the design of single electron device based novel digital logic circuits with the help of a Monte Carlo based simulator. A Single Electron Transistors (SET) is characterized by two most substantial determinants. One is very low power dissipation while the other is its small stature that makes it a favorable suitor for the future generation of very high level integration. With the utilization of SET, technology is moving past CMOS age resulting in power efficient, high integrity, handy and high speed devices. Conducting a check on the transport of single electrons is one of the most stirring aspects of SET technologies. Apparently, Monte Carlo technique is in vogue in terms of simulating SED based circuits. Hence, a MC based tool called SIMON 2.0 is exercised upon for the design and simulation of these digital logic circuits. Further, an efficient functioning of the logic circuits such as multiplexers, decoders, adders and converters are illustrated and established by means of circuit simulation using SIMON 2.0 simulator.

KEYWORDS

Coulomb Blockade, Single Electron Transistor (SET), tunnelling, Quantum Dot, Tunnelling Rate, CMOS, multiplexers, decoders, adders, Binary to Gray code converter, Gray to Binary Code converter, SIMON.

1. INTRODUCTION

One of the extraordinary creations of the 20th century is the semiconductor transistor. The last decade has seen a startling shrinkage in the feature size of MOS based circuits and an upsurge in the number of transistors. CMOS technology had a supremacy over the decades as bestowed by Moore's Law. As a result, the integration scale will be confined since power consumption will rise above the cooling limit [1]. The SED operation relies on a unique phenomenon called Coulomb Blockade which occurs in nanostructure and Gorter observed and studied this at a very low supply voltage [2]. The basic element of a single electron transistor is the tunnel junction [3]. As opposed to a MOSFET, the current conduction in a SET is regulated by the quantum mechanical tunnelling of electrons through the tunnel barrier. SET has immense potential for the evolution of future pint sized circuits as work has already been carried out for the evolution of set logic gate families [4], adders [5],[6], PLAs [7] etc. In this paper, Section II presents a brief description of MOSFET [8] and scaling limits [9]. In Section III, a review on SET is provided. Section IV deals with Coulomb Blockade [10] and orthodox theory whereas Section V provides an insight into the design and simulation results of different digital circuits utilizing MC [11] based simulator SIMON 2.0 [12].

2. MOSFET

MOSFET became the chief microelectronic device because it proved to be an essential building block of VLSI circuits. A MOSFET can be defined as a device consisting of four terminals i.e. drain, source, gate and bulk (see Figure 1).

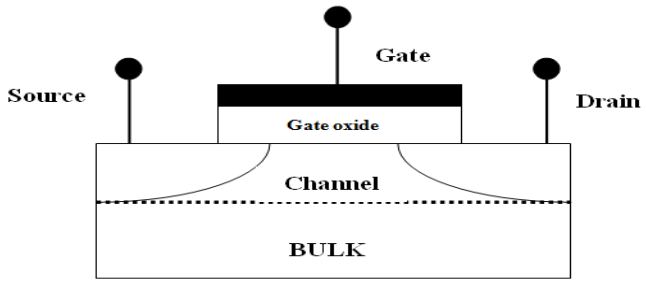


Figure 1: Generic MOSFET [13]

The MOSFET is primarily used as a switch in digital circuits. Its working can be demonstrated in the manner that the source and drain are two ends of the switch and the gate controls the turning ON & OFF of the channel. The gate terminal uses an electric field to control the conduction through the channel. The gate is insulated from the channel by a delicate layer of silicon dioxide. MOSFETs can be classified into types: nMOS and pMOS. They basically differ in the voltages that turn on the switch. Either type of the MOSFET is dependent on the element used to dope the silicon. In an nMOS transistor, an n-type material like Phosphorus is utilized to heavily dope the drain and source, while a p-type material is used to lightly dope the channel. On the other hand, in a pMOS transistor the drain and source are p-type and the bulk and channel are n- type. The MOSFET also has the ability to segregate the input from the output (gate to source or drain) which is an inclusion to its potential to implement logic. This ability of the MOSFET entitlesit to illustrate gain. Since a signal passes through a large number of transistors presuming that a little voltage is obscured at each transistor, then eventually the signal will deteriorate. The MOSFETs can be utilized to incorporate further intricate layout, which is another crucial feature of MOSFETs.The most common logic family, CMOS (Complementary metal-oxide semiconductor), adopts complimentary nMOS and pMOS transistors to frame logic gates such as inverters and NAND gates. Advances in the field of electronics have chaperoned to further retrench the size of the MOSFETs applied in integrated circuits. The decrease in size of the transistors also makes each one of them swift and they dissipate less power. The transistors become faster because there is a drop in the capacitance and boost in current. The increase in current can be visualized from the current flow equation for a transistor, when the gate voltage is at its highest value [13]. The current through the channel is given by the equation (A first order approximation):

$$I_D = \mu C_{OX} W/2L \, (V_{GS}-V_{th})^2 \qquad (1.1)$$

The above equation illustrates how different criterions of the MOSFET influence its behavior.
An upsurge in power consumption mainly through leakage currents, decreased tolerance for process variation and roaring costs are some of the aspects that affect the MOSFET scaling (decrease in size). Merely shrinking the size of the gate length and width will not lead to proper scaling but also demands a shortening of all the other dimensions; covering the gate/source and gate/drain alignment and the oxide thickness and depletion layer widths . When we scale down the depletion layer width it also indicates the need to scale down the doping density. There are two types of scaling listed below which are frequently used. One is constant field scaling and the other is constant voltage scaling. When the channel length of a MOSFET device is of same order

of magnitude as the depletion layer widths of the source and drain junction, the MOSFET device is considered to be short [14]. Assuming the channel length to be L; when the channel length L is reduced, the operation speed as well as the number of components per chip increases. In lieu of increasing the operating speed and the number of components, the problem of short- channel effect arises. The short channel effect is marked by two physical phenomena. They are as under: First, the shortcomings of the electron drift characteristics in the channel. Second, the shortening of the channel length results in the alteration of the threshold voltage.

3.SINGLE ELECTRON TRANSISTOR

We can characterize a Single electron transistor as a three-terminal, nano-electronic, tunnel junction device which utilizes a capacitively-coupled input voltage to modulate a drain-source current aiding as the amplifier output [15]. The tunnel junction is the chief element of a single electron transistor. The electric charge passes through the tunnel junction as multiples of e, given tunnelling is a discrete process [16].

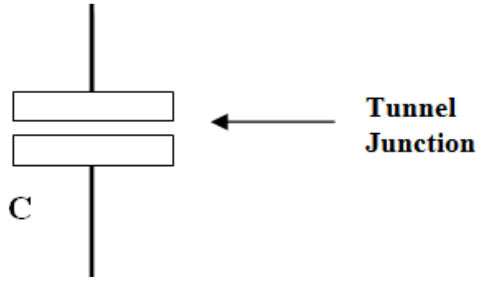


Figure 2: Tunnel Junction [17]

Further, when two tunnel junctions are laid down in series configuration, the fundamental construction of a single electron device can be obtained. The piece of conductor sandwiched between the two tunnel junctions is generally recognized as the island. It may also be called grain or a dot.

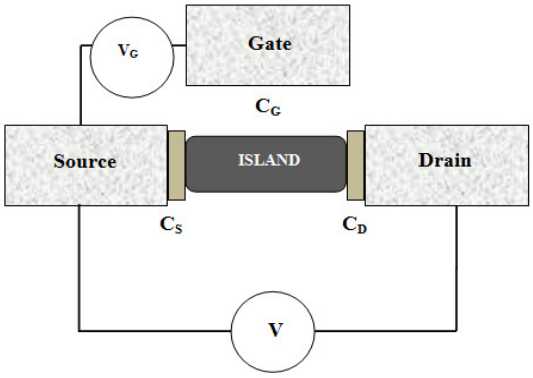
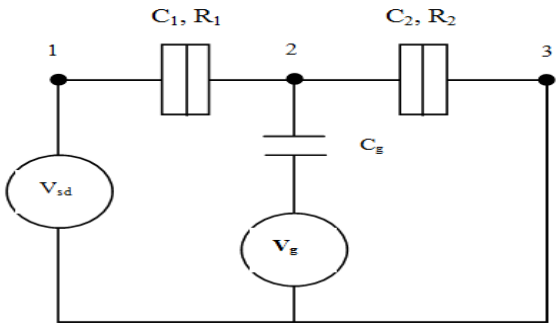


Figure 3: Structure of SET [18]

In Simple words, we can deliberate SET as a circuit that subsist of islands which are promptly connected with tunnel junctions and capacitors in conjunction with ideal voltage sources which control the circuits. In these devices, since $k_BT<<E_{cmin}$; the operating temperature (T) is diminished. Here E_{cmin} is the minimum charging energy. The minimum charging energy is also identical to the energy level spacing of the island[19]. In the above equation k_B is the Boltzmann constant. The minimum charging energy can be written as:

$$E_c = e^2/2C_\Sigma \qquad (1.2)$$

C_Σ is the total capacitance of the island. In other words, we can deliberate that the junction capacitance should be sufficiently small so as to reflect that the charging energy is higher than the thermal energy. Tunnel junctions, capacitances and voltage sources devise single electron circuits. Because of the stochastic nature of the electron tunnelling event, a tunnelling electron can be characterized as a discrete charge. We can note that in the Figure 4, the node 1 serves as the source electrode, node 2 & 4 behave as the island while node 3 again serves as the drain electrode. The regions between the nodes are the tunnel junctions which are defined by tunnel capacitance, C and tunnel resistance, R. Just as the bias voltage is zero the Fermi levels of both source and drain are in equilibrium, and it remains in equilibrium till there is some exertion of the bias voltage.



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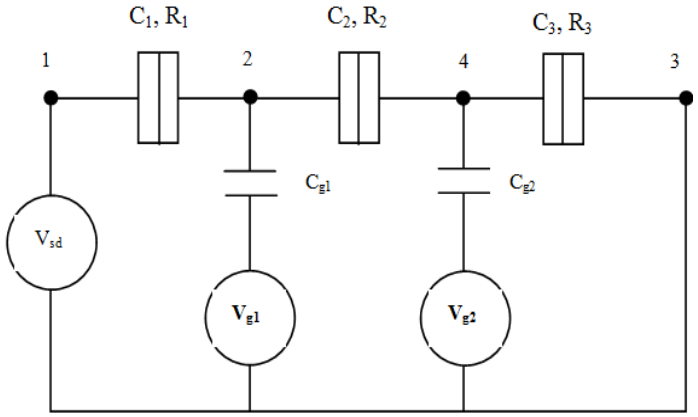


(b)

Figure 4 :(a) Equivalent circuit of SET consisting of tunnel and non-tunnel junctions with ideal voltage sources, (b) SET with double islands [17, 19].

There will be independent tunneling of an electron through the tunnel junctions from source to drain over the dot when an empty state is present at the energy level of the island that lies between the Fermi levels of the electrodes.

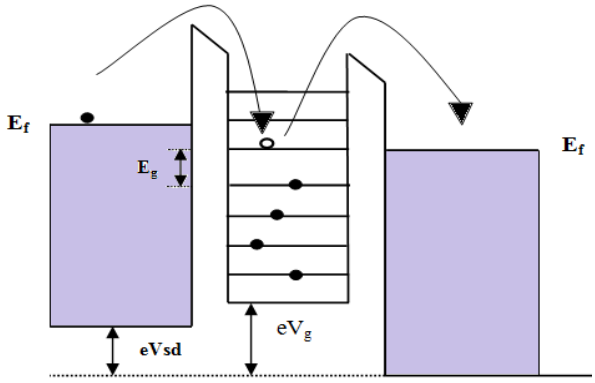


Figure 5: Schematic band diagram of Single electron transistor [19].

The electrostatic potential of the island is transformed by the electron tunnelling. The electron tunnelling also recasts the charge distribution in the circuit. As we modify the gate voltage various mannerisms of the circuit also changes them being the shifting of the energy levels, regulation on the addition and removal of electrons and turn on & off operations of the device. As opposed to a MOSFET, the current conduction in a SET is regulated by the quantum mechanical tunnelling of electrons through the tunnel barrier. A tunnel junction consists of two pieces of metal supported by a very thin (about 1 nm) insulator. Tunnelling through the insulator is the sole means for an electron to move from one metal electrode to the other [20]. Under some certain assumptions, since only one electron can travel from one terminal to another at a time, the device is commonly known as a SED (Single electron device). Charge transport is of discrete nature in a SED and is continuous in case of a MOSFET.

4. COULOMB BLOCKADE

Let us try to understand this phenomenon of coulomb blockade with the help of a small example. Let us assume a small spherical electro neutral conductor having capacitance C. The electron addition energy (E_A) is the amount of work that has to be done in order to add an extra electron to the spherical electro neutral conductor. Therefore, E_A can be written as:

$$E_A = E_C + E_K \approx E_C \approx e^2 / C \qquad (1.3)$$

Where E_C is the charging energy and E_K is the quantum kinetic energy respectively. Normally when the feature size is found to be more than 1nm; the quantum kinetic energy, E_K is omitted. Subsequently, the electrons in a single electron system require a minimum energy to tunnel through the barrier. When the applied external biases are unable to provide this energy, an electron cannot tunnel through. The device then goes into an OFF state. Such a condition is the Coulomb Blockade. The minimum energy required by the electrons to tunnel through can also be acquired from the existing thermal energy sources. Hence, to avoid the tunnelling of electron owing to the thermionic emission, the charging energy of the island capacitance has to be substantially higher than the existing thermal energy, K_BT. This can be written as:

$$(e^2/C)/k_BT > \beta \qquad (1.4)$$

T represents the room temperature whereas K_B is the Boltzmann's constant. The sum of all the device capacitance gives the total capacitance of the QD. This can be written as:

$$C_T = C_G + C_D + C_S \qquad (1.5)$$

It is also observed that the SET device operable at room temperature requires exceptionally demanding nanofabrication technology. A simple but productive orthodox theory has played an exclusive guiding role throughout the history of Single electronics. Kulik and Shekhter [21] had established the theory for a particular case study which was expanded for general systems by Averin and Likharev [22, 23]. This theory developed by Kulik and Shekhter, is based on the following assumptions. The electron energy spectrum is continuous, within the island. This particular assumption is valid for $E_k << k_bT$. Here Ek and $E_c$define the electron kinetic energy and charging energy, respectively [24]. Analogizing with other time scales, the time taken by the tunneling of electrons over the barrier (τ_t)is deemed negligible.For a SED of factual interest the assumption that τ_t must be 10^{-15} seconds holds true. It has to be noted that coherent quantum processes involving various concurrent tunneling events or cotunneling have been defied. This particular assumption holds true only under the event where electrons are effectively confined in the island.When tunnel resistances are larger than the fundamental resistance R_q, the confinement of the electron states within the islands can be ensured. The fundamental resistance is given as under:

$$R > R_q = h/e^2 = 25.813\Omega \qquad (1.6)$$

The QD (quantum dot) is connected to the source and drain electrodes through tunnel barriers. The gate electrode steers the potential in the Quantum Dot which is also capacitively coupled to the Quantum Dot [25].The gate voltage (Coulomb Oscillations) systematically modulates the current through the dot. The number of electrons is fixed when the current is zero. To limit the electrons in the Quantum Dot, the tunnel junction resistances must be greater than the quantum resistance (25.8 kΩ).The rates of all the possible tunnel events has to be resolved in order to mirror the tunneling of electron from island to island in a single electron circuit. The circuit's free energy changes as a result of a tunnel event.This change in the free energy decides the rate at which a tunnel event would take place.The difference between the electrostatic energy stored and the work done by the voltage sources of the circuit; denoted by U and W respectively can be expressed as:

$$F = U - W \qquad (1.7)$$

The tunneling rate of a tunnel event can be expressed as:

$$\Gamma = \frac{\Delta F}{e^2 R_T \left(1 - e^{-\frac{\Delta F}{kT}}\right)} \qquad (1.8)$$

ΔF here represents the change in the free energy as a result of the tunnel event, the tunnel junction resistance over which the electron is conducted is given by RT; kT is the thermal energy (k being the Boltzmann's constant and T is the temperature.

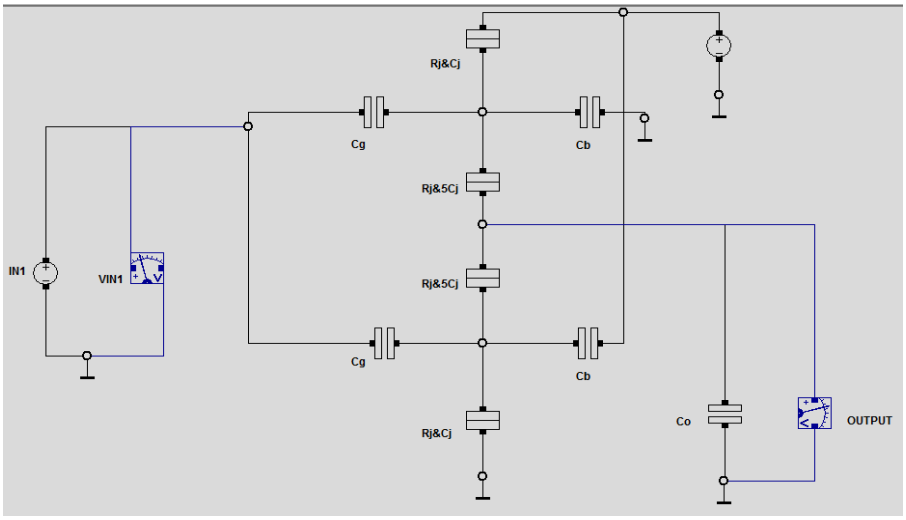
5. SIMON

A Monte Carlo based simulator for single electron circuits and devices is available and is named "SIMON". This simulator helps to report many of the design catechisms that arise. Basic features like graphical user interface and graphical circuit editor caters for and easy and error free handling of the simulator [26]. Circuit units like the tunnel junctions, capacitors, voltage sources and measuring devices for voltage, current and charge can be connected subjectively and all it requires is a mere mouse click. A few new features have been appended in the software which are: Stability plot, normal resistors, current sources, energy dependent density of states, and support for superconducting tunnel junctions, interactive single step mode, and Linux version without need for third party tools. We can simulate co-tunnelling with a simple Monte Carlo method. Most importantly, with SIMON we can confer about the crucial random problems like

background charge coupled with some possible solutions. We are considering single electron tunnel circuits which consists of islands connected randomly to tunnel junctions and capacitors and are impelled by voltage sources. The internal resistance of the voltage source is zero and hence it is deemed ideal. This work presents the design, simulation and analysis various digital circuits using SET. SIMON 2.0 is used to simulate the logic operation of gates, multiplexers, decoders, adders and converters.

5.1 Inverter

The basic building block of SET technology is the inverter that has noticeable alikeness to standard CMOS logic. The single electron inverter is shown in Figure 6, where five islands are hitched by four tunnel junctions.



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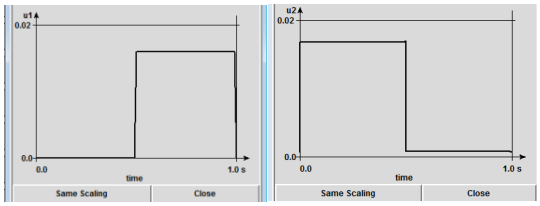
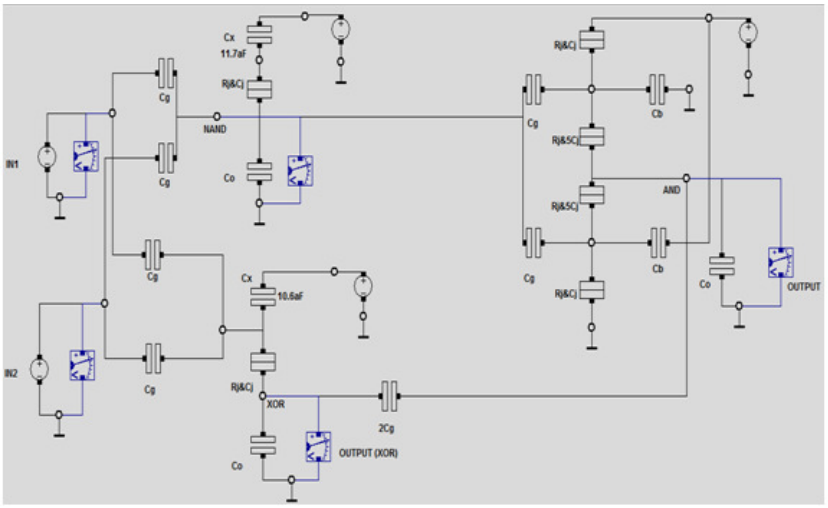


(b) (c)

Figure 6: (a)Single electron device based Inverter (b) Input waveform of Inverter (c) Simulation results of Inverter

5.2 Xor Gate

The XOR gate also marked as Exclusive ORgate or an inequality detector is a digital logic gate that devices an exclusive or operation. This means that a true output follows up if one, and only one, of the inputs to the gate are true. If either inputs are false or both are true, a false output follows. The Single electron XOR gate is shown in Figure 7 below.



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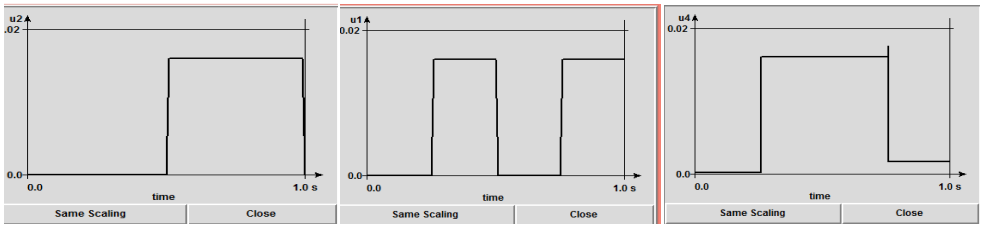
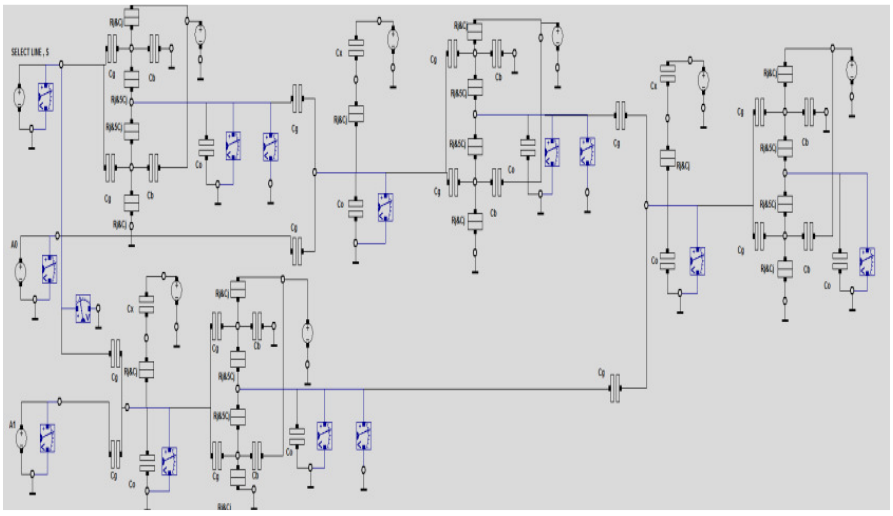


(b) (c) (d)

Figure 7: (a) Single electron device based XOR Gate (b) Input 'A' of XOR Gate (c) Input 'B' of XOR Gate (d)Simulation results of XOR Gate

5.3 2:1 Multiplexer

A Multiplexer is a combinational logic circuit. It can also be written as MUX or MPX. Depending on the application of a control signal, it can be used to switch one of several input lines through to a single common output line. The SET based 2 to 1 line multiplexer is shown in the figure below.



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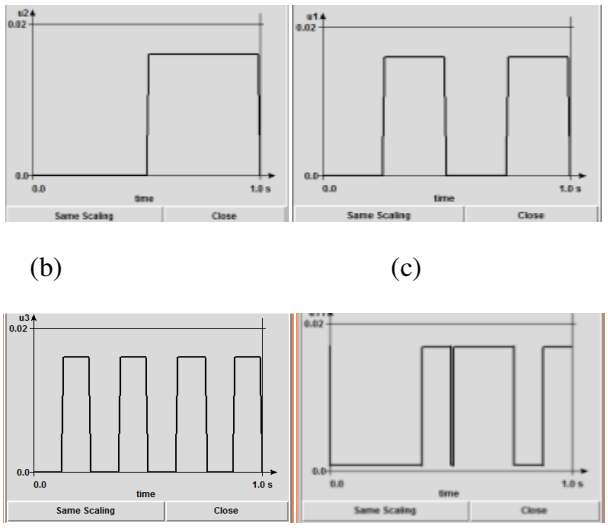


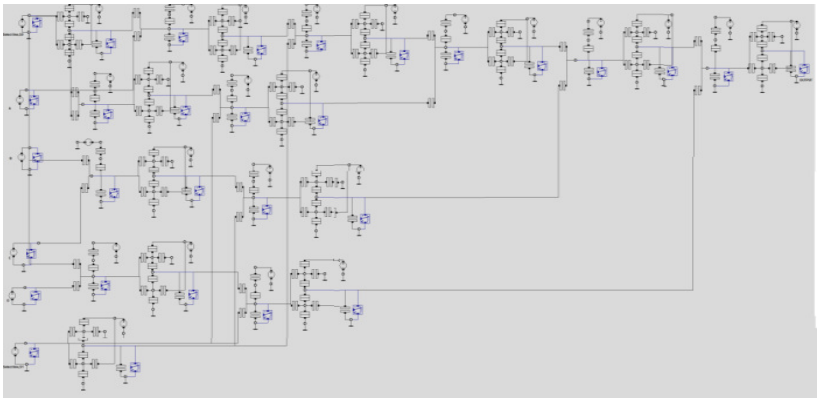
(b) (c)

(d) (e)

Figure 8: (a)Single electron device based 2:1 Multiplexer (b) Input waveform 'A0' of 2:1 Multiplexer (c) Input waveform 'A1' of 2:1 Multiplexer (d) Select Line, 'S' (e) Simulation results of 2:1 Multiplexer

5.4 4:1 Multiplexer

A logic circuit that picks one data line from amidst many is a multiplexer. They are often referred to as data selectors. A 4:1 line multiplexer illustrates how it channels out information from multiple data lines to one data line. The circuit for SET based 4:1 line multiplexer is shown in the figure below.



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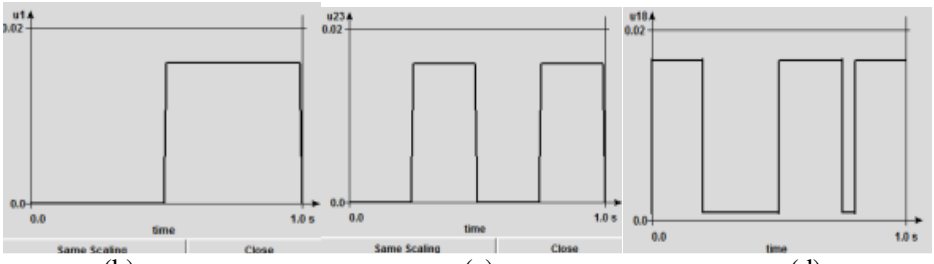
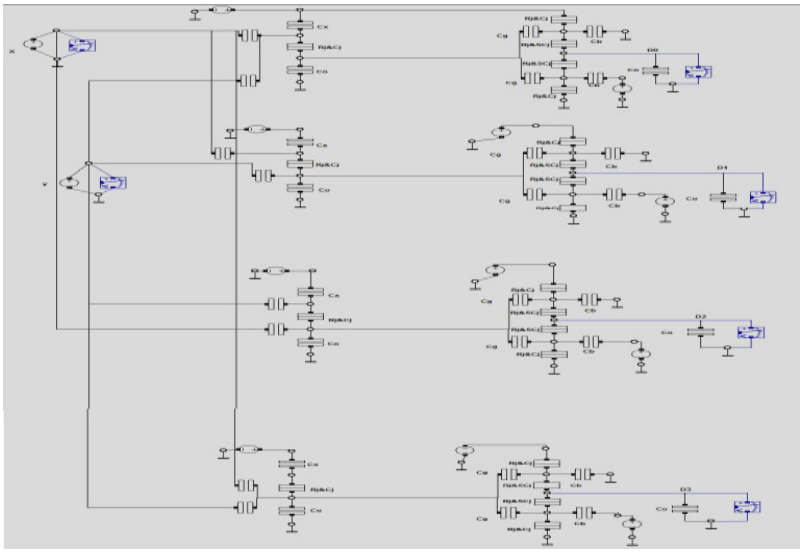


(b) (c) (d)

Figure 9: (a) Single electron device based 4:1 Multiplexer(b) Select line, S0 (c) Select line, S1(d) Simulation results of 4:1 Multiplexer.

5.5 2:4 Decoder

A decoder is one of the multiple input-output logic that allows us to obtain coded outputs derived from the coded inputs.Decoding is particularly essential in applications as multiplexing, memory address decoding.



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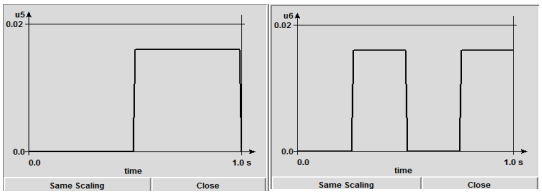

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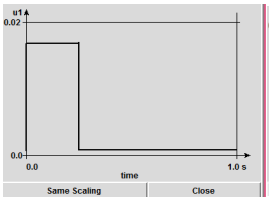

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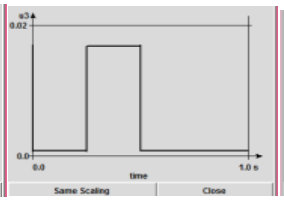

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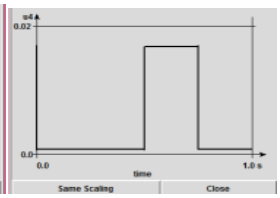

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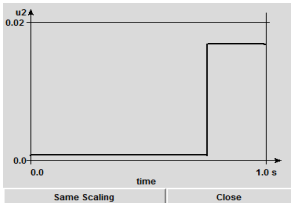
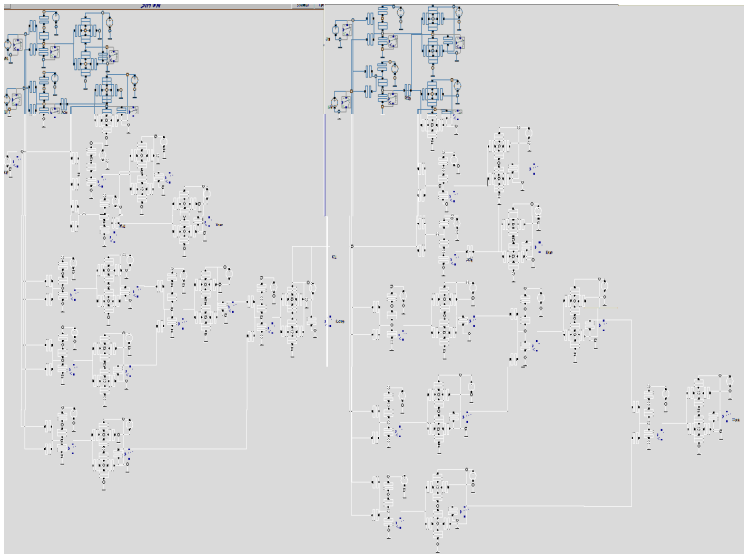


(g)

Figure 10:(a) Single electron device based 2:4 Decoder. Simulation results of 2:4 Decoder:(b) Input waveform ‘X’ (c) Input waveform ‘Y’ (d) Output waveform O0 (e) Output waveform O1 (f) Output waveform O2 (g) Output waveform O3

5.6 Parallel Adder

Another combinational circuit is the Parallel Adder which is not clocked or doesn't have a memory of its own. It does not have a feedback. It adds every bit position of the operands at the same time. Therefore, the number of bits to be added reflects the number of bit adders required. The Parallel Adder designed using SIMON 2.0 is as follows.



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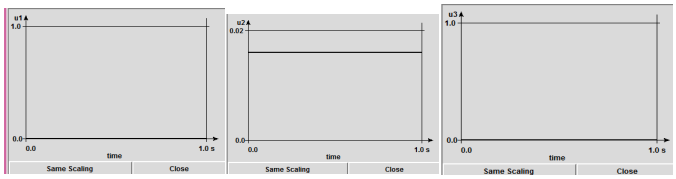
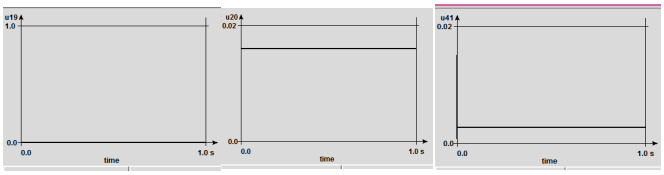
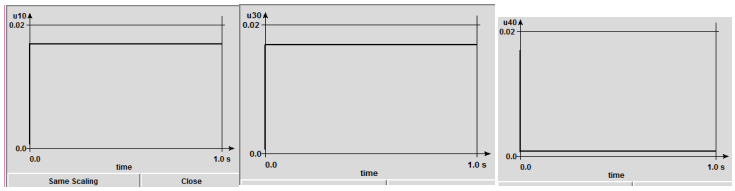


(b) (c) (d)



(e) (f) (g)

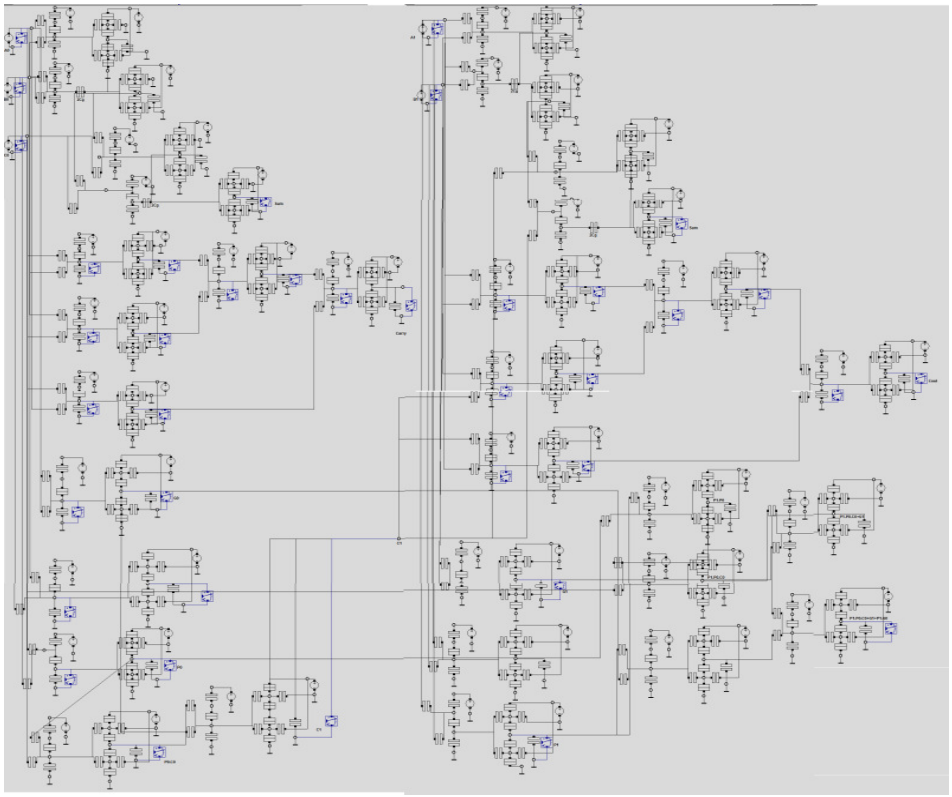


(h) (i) (j)

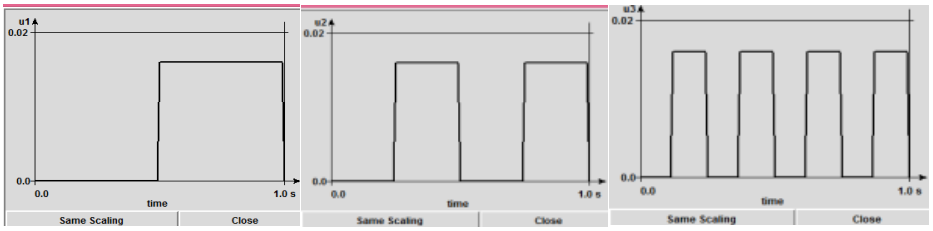
Figure 11: (a) Single electron device based Parallel Adder.Simulation results of Parallel Adder:(b) Input waveform A0 (c)Input waveform B0 (d) Input waveform C0 (e) Input waveform A1 (f) Input waveform B1 (g) Input waveform C1 (h) Sum Output waveform of first Full Adder, S0 (i) Sum Output waveform of second Full Adder, S1 (j) Output waveform Cout of Parallel Adder

5.7 Look Ahead Carry Adder

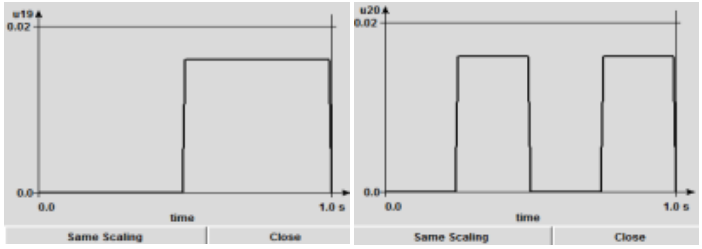
Another type of adder used in digital logic is a look ahead carry adder also known as the fast adder. As opposed to a slower ripple carry adder, the speed of operation is improved by decreasing the amount of time needed to determine the carry bits. The single electron device based look ahead carry adder is shown below.



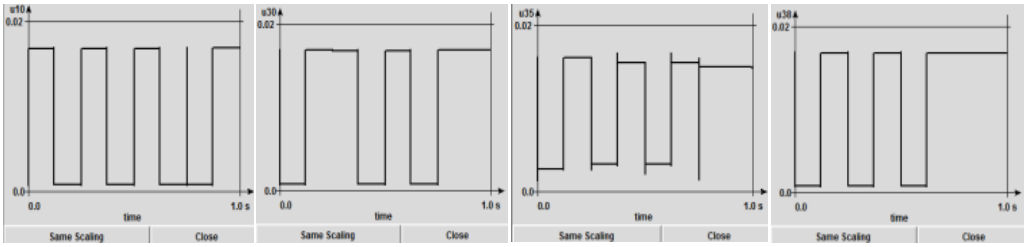
(a)



(b) (c) (d)



(e) (f)

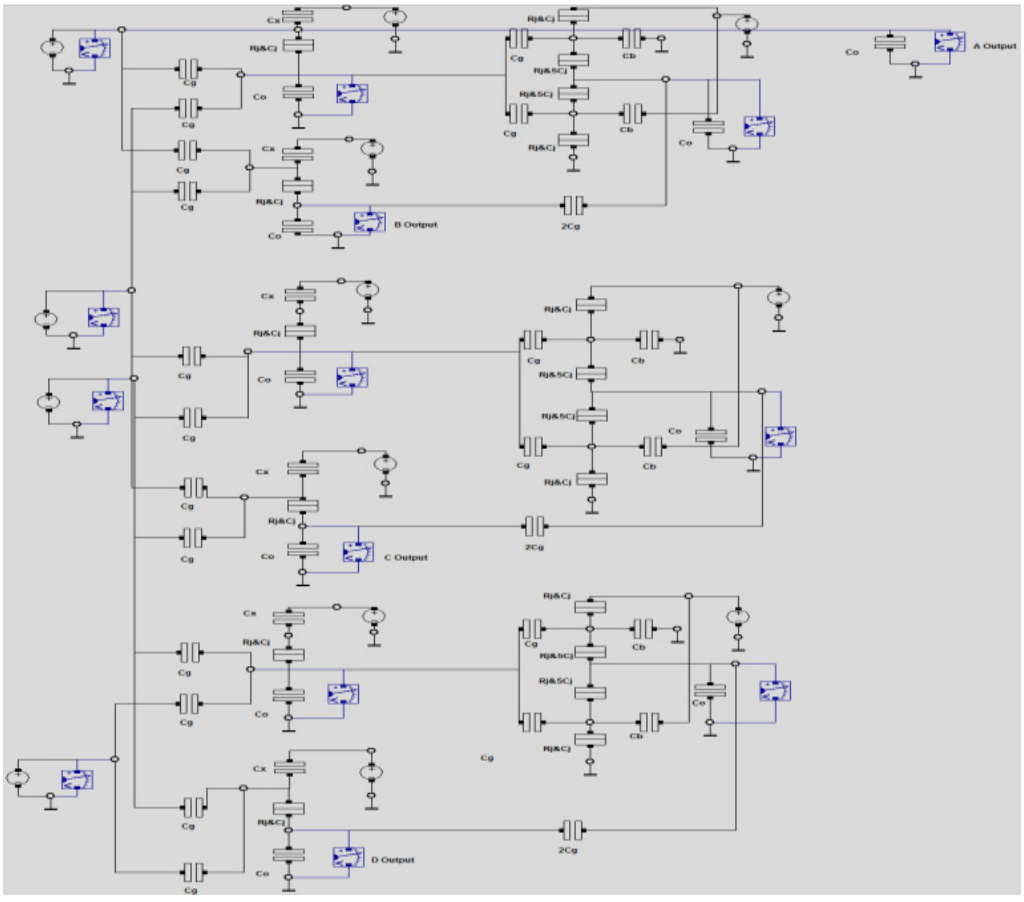


(g) (h) (i) (j)

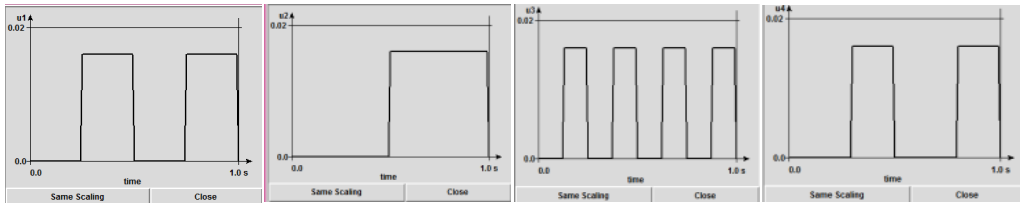
Figure 12: (a) Single electron device based Look Ahead Carry Adder.Simulation results of Look Ahead Carry Adder: (b) Input waveform A0 (c) Input waveform B0 (d) Input waveform C0 (e) Input waveform A1 (f) Input waveform B1 (g) Output waveform S0 (h) Output waveform S1 (i) Output waveform C1(j) Output waveformC2 of Look ahead carry adder.

5.8 Binary to Gray Code Converter

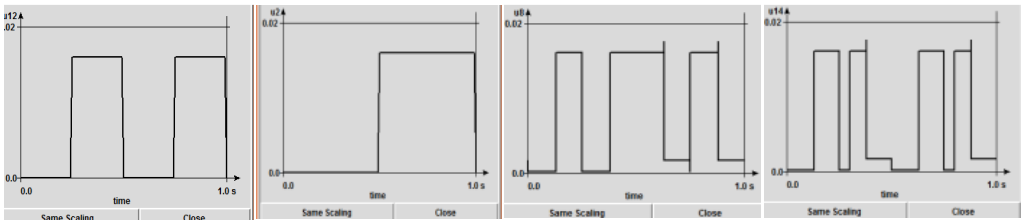
The text or data that the computers or other devices bear is staged by a binary code. The text or data is personified as a sequence of zeroes and ones. Gray codes are essential as they find a plenty of application in analog as well as digital converters. Two adjacent code numbers can be distinguished from each other by just one bit. The single electron device based binary to gray code converter is shown in the figure below.



(a)



(b)(c)(d)(e)

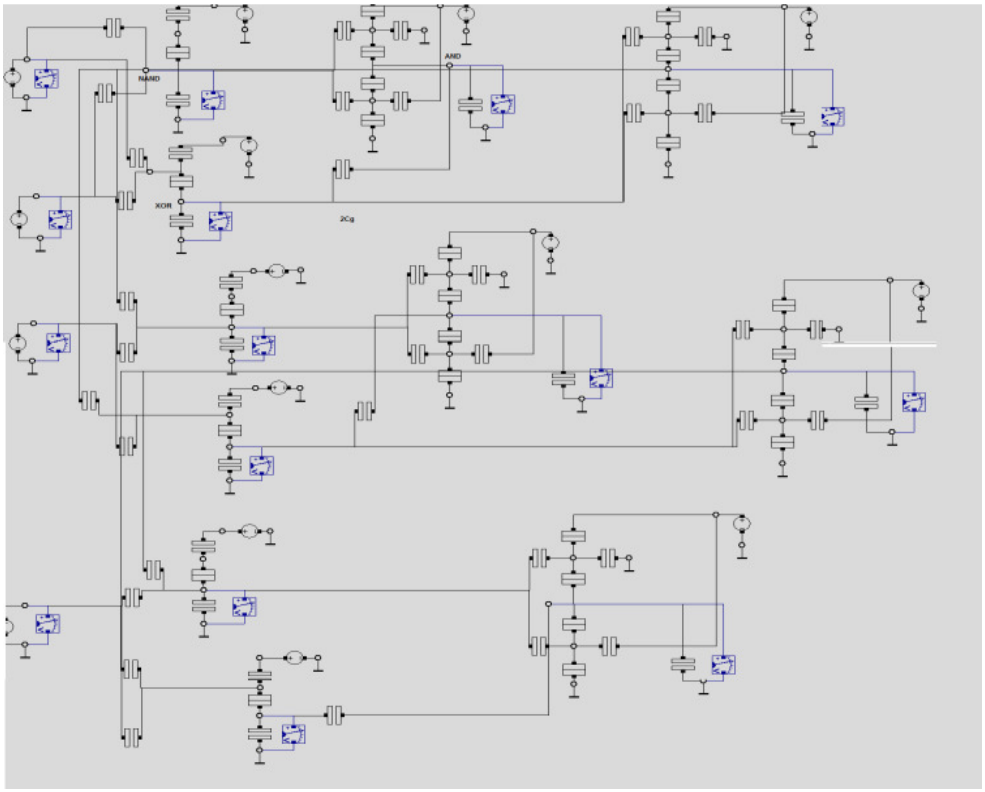


(f)(g)(h)(i)

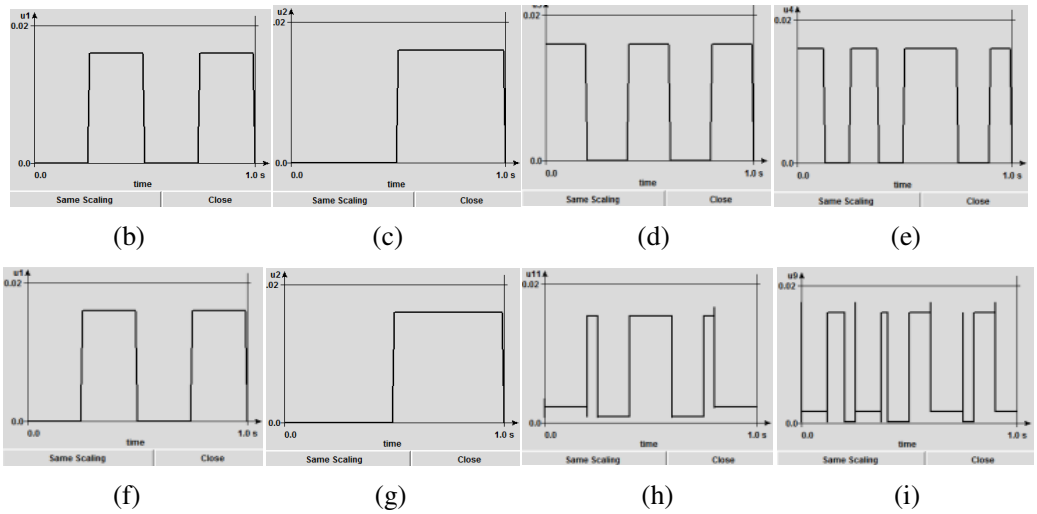
Figure 13: (a) Single electron device based Binary to Gray Code Converter. Simulation results of Binary to Gray Code Converter :(b) Input waveform W (b) Input waveform X (c) Input waveform Y (d)Input waveform Z (e) Output waveform A (f) Output waveform A (g) Output waveform B (h)Output waveform C (i) Output waveform D

5.9 Gray to Binary Code Converter

This circuit performs the gray to binary code conversion and has been designed using single electron device as shown below.



(a)



(b) (c) (d) (e)

(f) (g) (h) (i)

Figure 14:(a)Single electron device based Gray to Binary Code Converter.Simulation results of Gray to Binary Code Converter : (b)Input waveform W (c) Input waveform X (d) Input waveform Y (e) Input waveform Z (f) Output waveform A (g) Output waveform B (h) Output waveform C (i) Output waveform D.

6. CONCLUSION

In this paper, the design and simulation of novel digital circuits have been presented. The design and simulation has been accomplished using a Monte Carlo based tool for single electron circuit simulation named SIMON 2.0. The outputs of the digital circuits have been verified. The work was started off with the designing of the basic logic gates and its functional attributes were substantiated. This work can be stretched out to build bigger circuits where we can explore the possibility of large scale integration that runs on very low power. Further this work can also be drawn out to design subsystems. Accuracy is assured when using the Monte Carlo method but the process experiences a setback in terms of time efficiency while simulating large circuits.SETs are known to run on very less current and hence exhibits low power dissipation. On the other hand CMOS functions at realistic temperatures. Therefore, SET-CMOS circuits can be fabricated with the help of another MC based simulator called SMARTSPICE offering better accuracy.

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