A SINGLE-ENDED AND BIT-INTERLEAVING 7T SRAM CELL IN SUB-THRESHOLD REGION WITH A SMALL AREA CONSUPTION

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ABSTRACT

In recent years, to reduce power consumption and increase cell resistance against soft error, several sub-threshold SRAM cell have been provided. Also, in the memory design, to increase the memory density and reduce the occupied area, sub-100 nm technologies have been used. These technologies also increase the sensitivity of the cell against soft error. Among the proposed methods to confront soft error, bit-interleaving structure is one of the most successful methods. But the designed bit-interleaving cells usually have many transistors in order to achieve the ideal features. Moreover, another problem in the bit-interleaving cells is half-select issue. In this paper, a single-ended sub-threshold cell is presented. This cell has been designed in multi-Vt 32nm technology. On the other hand, the suggested cell can be implemented in the bit-interleaving structure to confront soft error. In the cell, 7 transistors have been used while the cell is without half-select problem. Simulations show the suggested cell has less power consumption compared with standard 6T and other bit-interleaving cells. Also, in the proposed cell, write margin and write time delay are better than the under comparison cells, while the suggested cell stability in read and hold modes and read time delay are also optimal.

KEYWORDS

Sub-threshold SRAM, Bit interleaving, Half-select, Boosted voltage, Multi Vth transistor

1. INTRODUCTION

One of the most important elements of the chip is 6T SRAM memory. Figure 1 shows the standard 6T SRAM cell. This memory has a high power consumption. One of the most effective methods for reducing power consumption in CMOS circuits is reducing supply voltage (VDD) [1]. But reducing supply voltage and using of smaller technologies in the memory circuits in order to increase the density lead to reducing cell stability (or static noise margin), increasing read and write failures and reducing cell resistance against soft error [2]. Soft error is generated by alpha particles and neutrons. These particles, after collision with the sensitive nodes of the circuit (storage nodes Q and QB), change the data stored in these nodes [3-6]. By reducing the power supply and the dimensions of the transistors, the circuit becomes more sensitive to soft error and the failures caused by these particles are increased. One of the most successful methods to confront soft error is bit-interleaving architecture. But the designed bit-interleaving cells usually have many transistors in order to achieve the ideal features. Therefore, the designed cell occupies a large area. On the order hand, another problem in the bit-interleaving cells is half-select issue [7-9].

In recent years, several sub-threshold SRAM cell with bit-interleaving structure in sub-100 nm technologies have been proposed. For example, 7T, 10T and 12T cells have been presented in [10-12]. The cells have been designed in sub-threshold region and sub-100 nm technologies in

order to reduce power consumption. These cells are in bit-interleaving architecture in order to confront soft error. But simulation results show 7T cell stability in [10] is low in read mode (The most sensitive mode). The 10T and 12T cells in [11, 12] have ideal features but in their design have been used many transistors which lead to increasing area and reducing density.

In this paper, a sub-threshold bit-interleaving 7T SRAM cell in multi-Vt 32 nm technology has been designed. The proposed cell has ideal features like low power consumption, high stability and write margin, low delay, high speed and small area compared to other bit-interleaving cell while the proposed cell has been designed with 7 transistors and is without half-select problem.
The rest of this paper is organized as follows. Section 2 describes conventional 6T SRAM cell and its problems in sub-threshold region and advanced technologies. Section 3 explains the proposed 7T SRAM cell in read, write and hold modes. In Section 4, simulation results are presented. In this section, the proposed cell has been compared with the standard 6T cell and the 7T, 10T and 12T bit-interleaving cells in [10-12]. The paper is concluded in section 5.

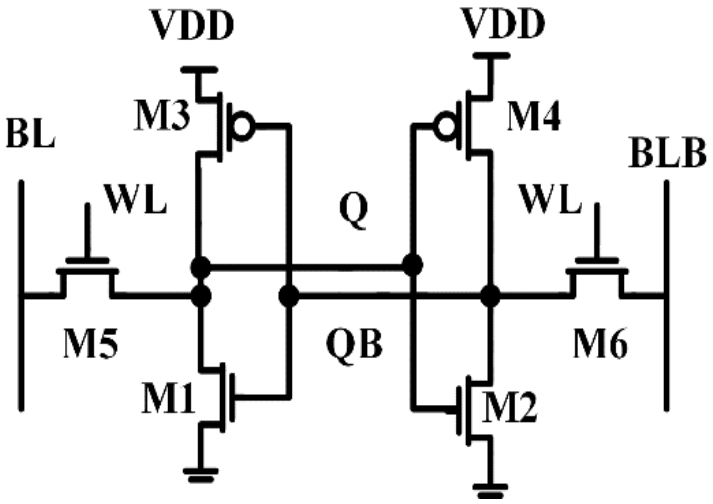

Figure 1. Standard 6T SRAM cell

2. THE STANDARD 6T SRAM CELL AND ITS CHALLENGES IN SUB-THRESHOLD REGION AND SUB- 100 NM TECHNOLOGIES

Figure 1 shows the 6T SRAM cell. This cell contains two inverters and two access transistors. In the cell, M1 and M2 transistors are driver transistors. M3 and M4 transistors are load transistors and M5 and M6 transistors are access transistors. Q and QB nodes are storage nodes. Suppose that in this cell, the Q and QB nodes are 0 and 1 logic, respectively. In reading mode, BL and BLB are precharged to VDD and WL is also equal to 1 logic value. By turning on the M5 and M6 transistors, BL node capacitor is discharged through M1 and M5 and BLB node capacitor remains at VDD. Then the 0 and 1 values are moved to output ports. In writing mode, new data is placed on BL and BLB and WL is also equal to 1 logic value. By turning on the M5 and M6 transistors, the new data in BL and BLB is transmitted to Q and Q nodes. In holding mode, BL and BLB are precharged to VDD to be ready for next reading operation and WL is equal to 0. As you can see in Figure 1, the Q and QB nodes are the input and output of the inverters. In holding mode, when the M5 and M6 transistors are off, the Q and QB nodes drive the inverters and thus the data is retained in the cell.

In the 6T cell design, the transistor dimensions should be as follows [1, 10]:

Driver transistor > access transistor> load transistor

In order to have the correct read operation, the driver transistors should be stronger than the access transistors and to have the correct writing operation in the cell, the access transistors should be stronger than the load transistors. So determining the size of access transistors (especially in sub-threshold region) is difficult. Also, this cell has a high power consumption. The design of this cell in the sub-threshold region reduces the power consumption but reducing supply voltage leads to reducing cell stability, increasing read and write failures, reducing read and write speeds, increasing read and write delays and reducing cell resistance against soft error. On the order hand, using of smaller technologies in the memory circuits in order to increase the density has a negative effect on some of the above parameters such as stability, cell resistance against soft error, correct read and write operations.

3. THE PROPOSED 7T SRAM CELL

Figure 2 shows the suggested 7T cell. In this cell, the read operation runs from the left side and the write operation runs from the right side. M1, M2 and M3 transistors also hold data stored in Q and QB nodes.

3.1. Read Operation In The Proposed 7t Cell

In read mode, in the suggested 7T cell, we add M6 and M7 SVt transistors in order to increase cell stability. Then in order to increase read speed, we use boosted voltage (VDD+0.3 V) for read word line (RWL). In this mode, G1 = "0", RWL = "VDD + 0.3 V" and RBL is precharged to VDD. If QB = "0", then M7 turns off and RBL remains at the level of VDD. If QB = "VDD", then M7 turns on and RBL is discharged to "0" through M6 and M7 transistors.
In this mode, the M7 transistor isolates the QB node from the reading access transistor (M6 transistor). Therefore, the stability of reading mode (RSNM) is increased.

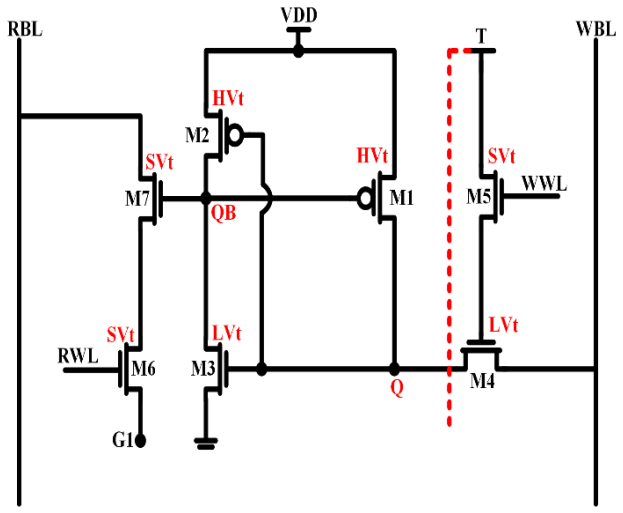

Figure 2. Proposed 7T cell

3.2. Writing Mode In The Proposed 7t Cell

According to Figure 2, in the proposed 7T cell, we eliminate M2 from Figure 1 in the write part of our new proposed 7T cell. In this case to reach fast accessible in write mode, we utilized low voltage transistor M4 (LVt M4) as write access transistor. Moreover to get a strong "0" in hold and read modes at node Q after writing "0", we use M1 as high voltage threshold (HVt) to decrease leakage current. Furthermore we set WBL to "0" in reading and holding modes to decrease the leakage current through M4 transistor to Q node.

Suppose Q has a "1" logic value and we want to write a "0" to Q. We set WWL and T to "VDD+0.3 V" and WBL to "0". In this situation, M4 transistor is on and a "0" logic value is written to Q through this transistor.

Now suppose Q has a "0" logic value and we want to write a "1" logic value to Q node. We set WWL and T to "VDD+0.3V" and WBL to "1" logic value. In this condition, M4 is on and Q node gives "1" logical value.in this mode, RWL and G1 give "0" and "1" logical values, respectively and RBL is in "1" logical value.

3.3. Holding Mode In The Suggested 7t Cell

In the hold mode, M6, M4 and M5 are turned off, and G1 is connected to "1". Also, in this mode, RBL is pre-charged to VDD and WBL is connected to "0" to have a strong "0" in node Q. Although write mode improves by removing the driver transistor, the cell strength is reduced to hold "0". For this reason, in the design of the 7T cell, multi Vt transistors are used. By using HVt transistors in pull up path and using the smallest size for this PMOS transistors, the leakage current injection to node Q is reduced.

3.4. Half-Select Problem In The Proposed Cell

In bit-interleaving SRAM cell design, half-select problem is center of attraction for the researchers. In writing mode, in the proposed 7T SRAM cell, M5 transistor is used. This transistor prevents the half-select problem. Figure 3 shows two cells of our memory array in writing mode. To write a value in the first cell, WWL is set to VDD+300mv, the first cell T is set to VDD+300mv by the first column address. At this time, the second cell in the first row is ready to be half selected, but due to the low value of the second column address, the second cell T is set to "0", as a result, M4 transistor turns off. Thus, the stored value in this cell is preserved.

3.5. Control Circuit In The Proposed Cell

We consider our proposed cell in a memory array according Figure 4. According to the figure, each column has a common control circuit which follows table 1 to produce an appropriate voltage in each mode. We design the control circuit as Figure 5. According to the design when cell is in read mode (read-en and CA="1") G1 and T are set to "0" logic value. When cell is in write mode (write-en and CA="1") G1 and T are set to "VDD" and "VDD+0.3v" respectively and when cell is in hold mode (read-en and write-en and CA="0") G1 and T are set to "VDD" and "0" respectively.

Table 1. G1 and T values in different modes

Modes	G1	T
hold	VDD	0
read	0	0
write	VDD	VDD+0.3V

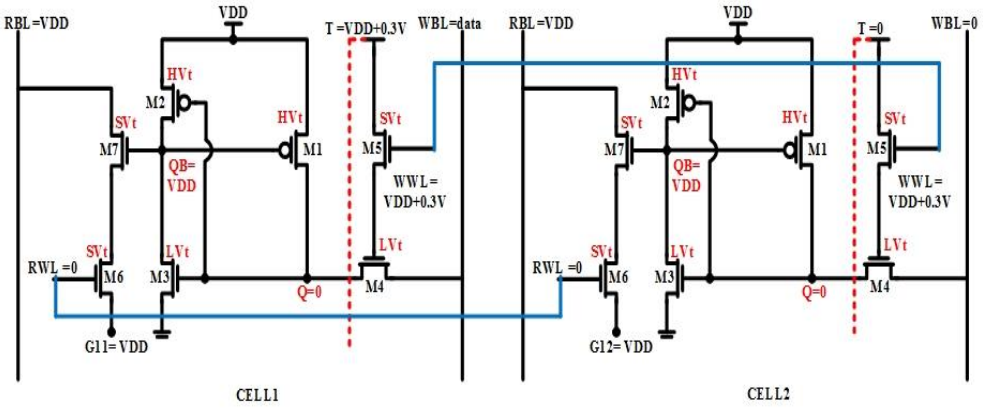

Figure 3. Two cells of our memory array in writing mode

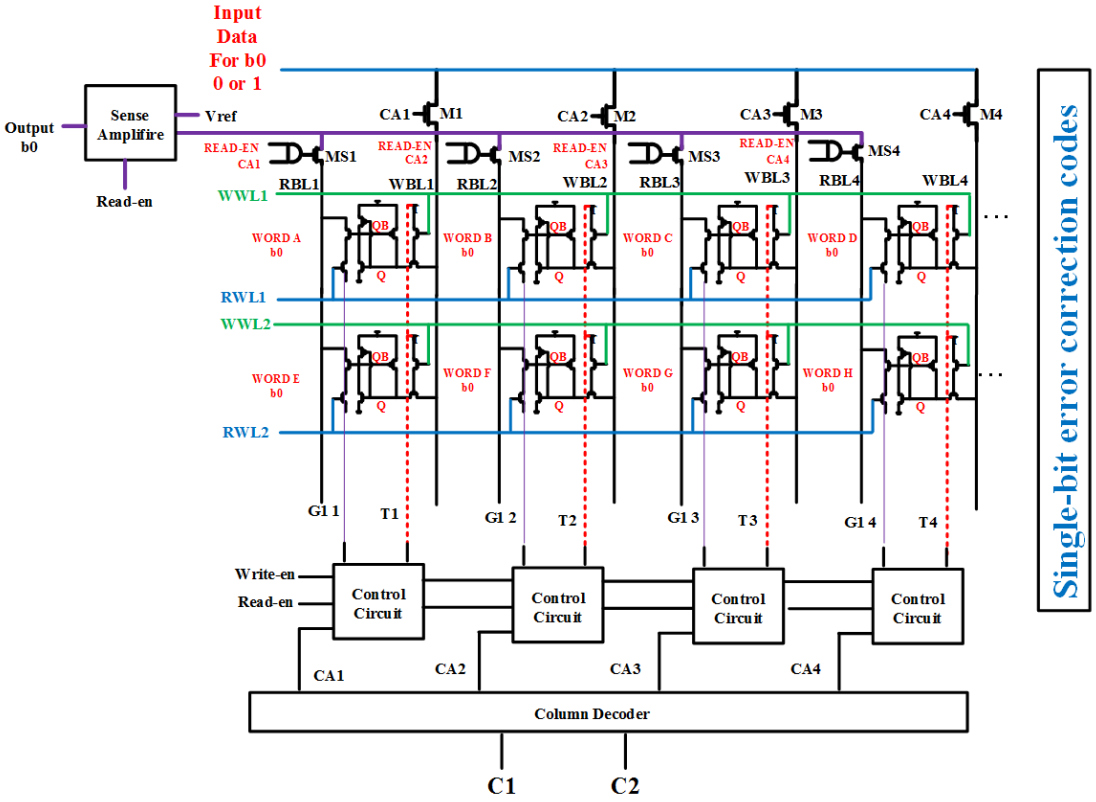

Figure 4. The Proposed 7T SRAM cell memory array

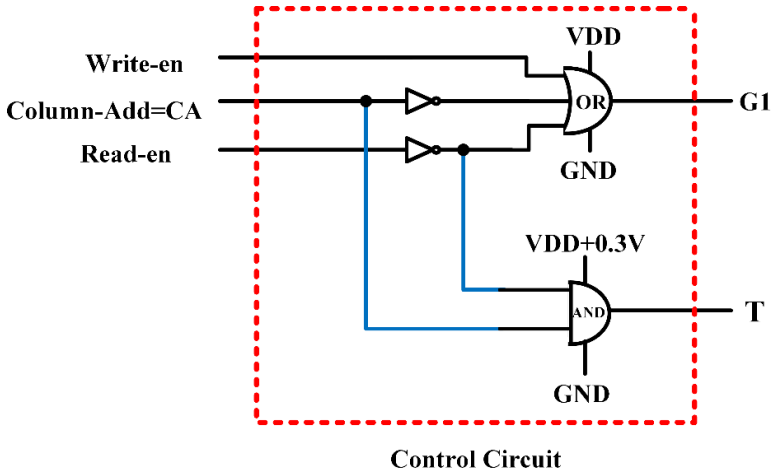

Figure 5. Control circuit

4. SIMULATIONS

The proposed 7T cell is simulated in 32 nm PTM technology [15]. We consider SVt, HP and LP models for LVt and HVt transistors in our simulation. The suggested 7T cell has been compared with the conventional 6T cell and the 7T, 10T, 11T and 12T [10-14] bit interleaving SRAM cells.

4.1. Hold And Read Static Noise Margin (Hsnm And Rsnm)

In order to analysis the cell stability of the SRAM memory in the read and hold modes, we can use the SNM. As mentioned in [16], The SNM value is obtained from the SRAM cell voltage transfer characteristic (VTC). To find the SNM of circuits we plot the butterfly diagram of them and try to put a square with maximum dimension in the plot. Value of this square leg is equal to SNM [15]. Figure 6 shows butterfly diagram of 6T and the suggested 7T SRAM cells in hold mode and VDD = 0.5 V. In this case, the access transistors are off and the large wings demonstrate the appropriate stability of these cells. We have run Monte Carlo simulations with 100 iterations in 5% Vt, thickness of gate oxide and channel length variations with Gaussian function in sigma 3 in order to model the deviations.

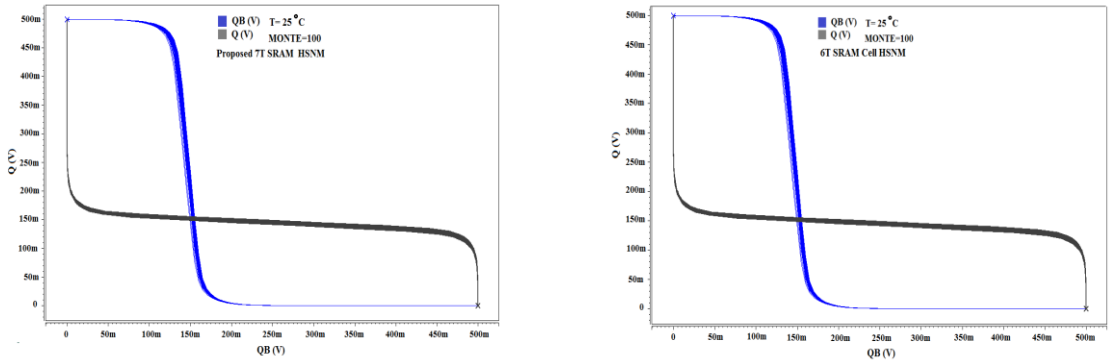

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Figure 6. Butterfly diagram in hold mode and VDD = 0.5 V a) proposed 7T cell b) 6T cell

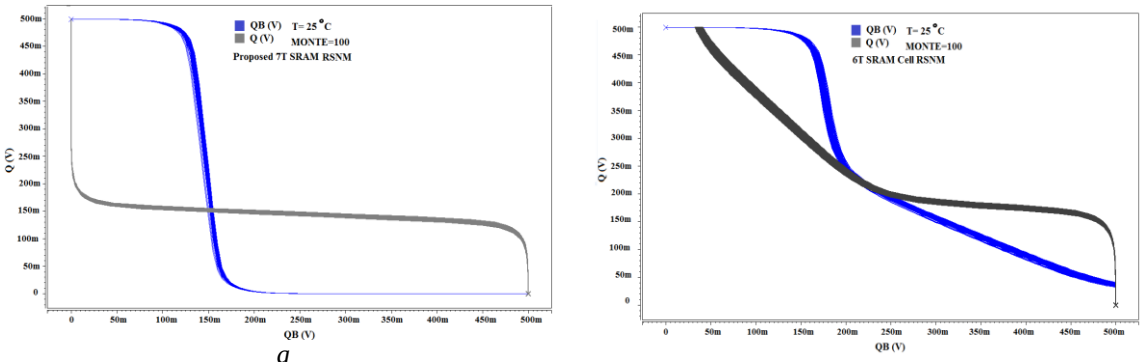

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Figure 7. Butterfly diagram in read mode and VDD = 0.5 V a) proposed 7T cell b) 6T cell

Figure 7 shows the butterfly diagram of 6T and 7T cells in read mode with VDD = 0.5 V. 6T SRAM cell read butterfly diagram wing is small. In this case, the access transistors are on and there are variations in threshold voltage. As a result, read stability for this cell in low voltages is unacceptable .On the other hand, read stability for the suggested 7T cell is equal to hold stability. Because, in this cell we use a buffer (transistor M7) and boosted voltage for word line (RWL). In fact in this mode, by using the buffer, storage node QB is isolated from read access transistor M6. Figure 8 shows HSNM and RSNM of under test SRAM cells in various VDDs.

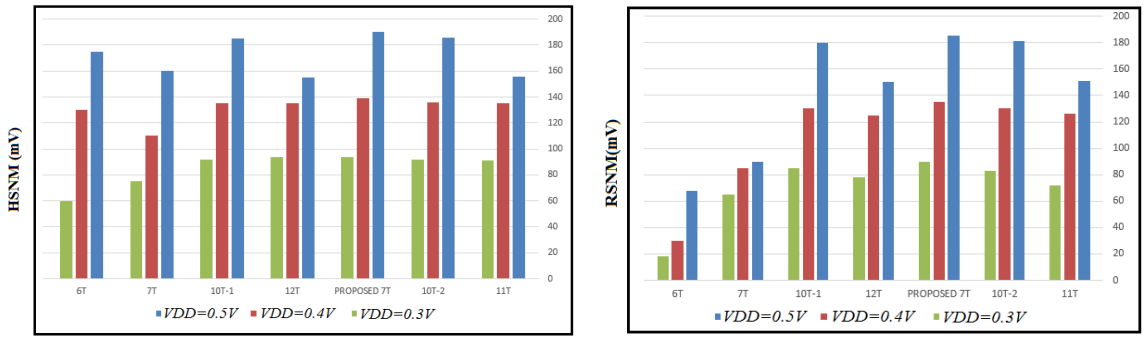

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Figure 8. a) Hold stability for various cells b) Read stability for various cells

4.2. Write Margin

In order to analysis the write ability in the SRAM cell, we used write margin (WM) parameter. To measure the write margin (WM) of different cells, the second method in [18] is considered. In this method, SRAM cell is configured in write mode (for a write '1' case). The voltage of BL (the bitline connected to the node holding '1' initially) is swept downward during simulation. The write margin is defined as the BLB value at the point when Q and QB flip. The WM of different cells versus supply voltage, is shown in Figure 9. We examined 100 MONTE CARLO simulations to model the variability.

In the proposed cell, owing to boosted write word line feature and removing driver transistor, write operation is more likely to succeed. Larger WM of the proposed cell in Figure 9 confirms this prediction.

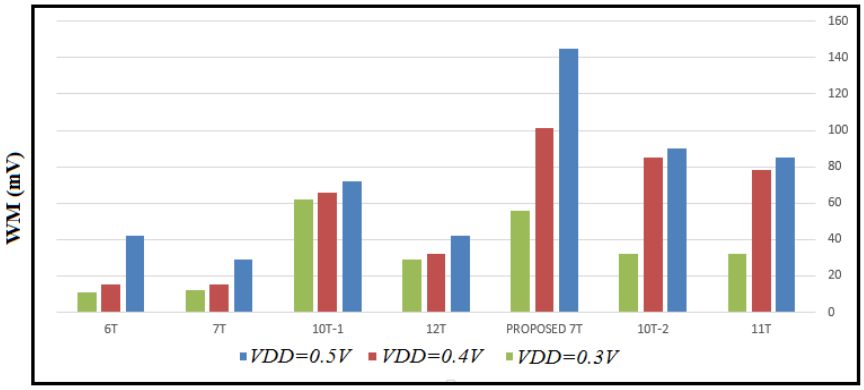

Figure 9. WM of cells in different VDDs

4.3. Speed Of The Cells

Figure 10 compares read-time delay and write-time delay for conventional 6T SRAM cell , proposed 7T SRAM cell and other counterpart cells in T = 25℃ and VDD = 0.5 V. Cell's write-time is defined as the time that takes between 50% of word-line (WL) when goes to Vdd and the time that voltages of the nodes of the cell become equal ("Q" and "QB). Cell's read-time is defined as the time that takes between activation of read word line and the time that 50 mV voltage difference occur between read bit-lines (or between read bit-line and Vdd rail in cells with single ended read operation). As shown in figure 10, due to using Multi-Vt transistors, removing driver transistor and boosted voltage, the suggested 7T cell write delay is lower than other cells while the cell read delay is also acceptable.

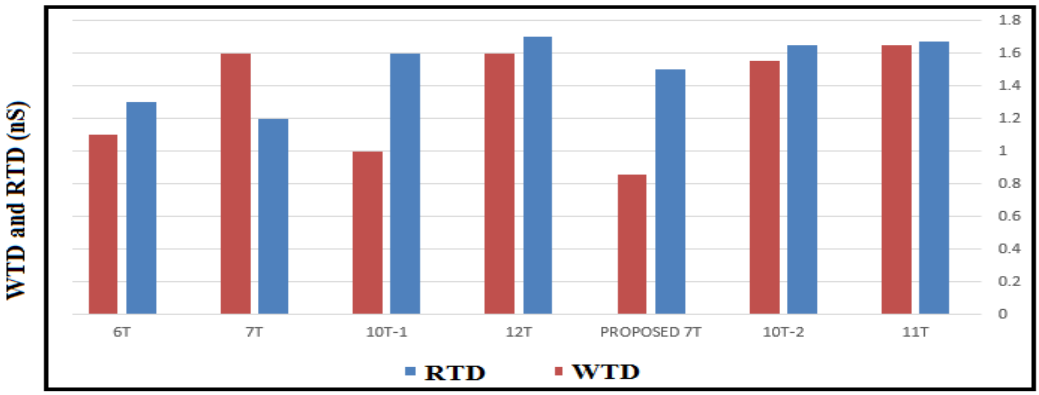

Figure 10. Delays for different cells in T = 25℃ and VDD = 0.5 V (nS)

4.4. Power Consumption

Tables 2, 3 and 4 show power consumption for various cells in read, hold and write modes, respectively. Read power consumption of the suggested 7T cell is nearly equal to the 7T cell in [10]. But our 7T cell has better features in sub threshold region such as better WM, RSNM, hold and write power and delay. As well as, generally, hold and write power consumption for the suggested 7T cell is lower than other cells.

Table 2. Read power consumption (nW)

VDD(V)	6T	7T	10T-1	12T	Proposed7T	10T-2	11T
0.3	34.9	2.4	5	6.3	0.032	5.5	6.7
0.4	353	27.1	59.2	78	32.47	61	66
0.5	1760	152	335	489	149.9	346	358

Table 3. Hold power consumption (nW)

VDD(V)	6T	7T	10T-1	12T	Proposed7T	10T-2	11T
0.3	0.21	0.052	0.02	0.3	0.007	0.021	0.023
0.4	0.357	0.093	0.04	0.5	0.015	0.039	0.042
0.5	0.595	0.164	0.07	0.9	0.032	0.076	0.08

Table 4. Write power consumption (nW)

VDD(V)	6T	7T	10T-1	12T	Proposed7T	10T-2	11T
0.3	1.3	0.6	0.39	0.45	0.05	0.4	0.42
0.4	2.1	1.22	0.778	0.9	0. 39	0.82	0.86
0.5	3	2.1	1.44	1.6	0.65	1.54	1.7

4.5. The Proposed 7T Cell Layout And Post-Layout Simulations

Figure 11 shows the layout of the suggested 7T cell in LEDIT software. In this design, λ is half of technology (technology is 32nm and λ is 16 nm). In proposed 7T cell design, the HP and LP model in [15] are used for LVt and HVt transistors. These transistors have the same layout design. This is because their difference is in threshold voltage and threshold voltage difference is caused by gate work function.

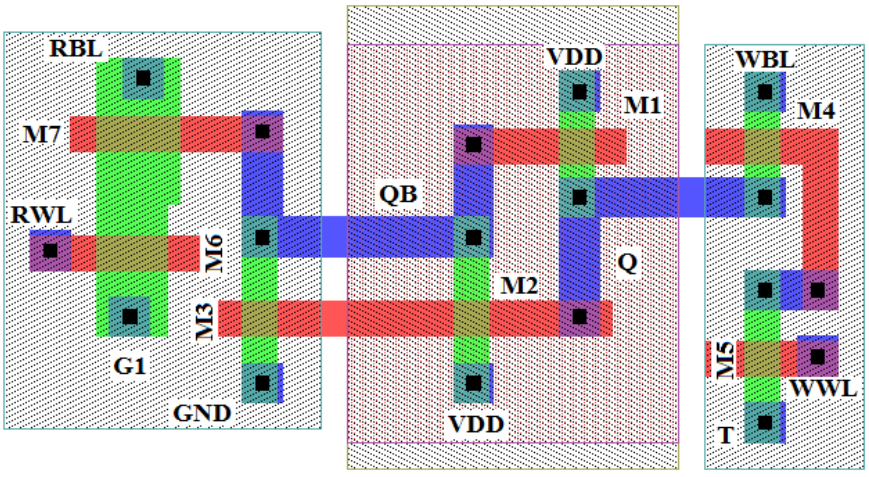

Figure 11. Layout of the suggested 7T cell

We run post-layout simulation by extracting net list of the layout. Tables 5, 6 and 7 show power consumption, HSNM, RSNM, WM, RTD and WTD for the proposed 7T SRAM cell for post-layout in different VDDs. As expected, by adding the parasitic capacitors, delays increase and the amounts of SNM and WM make a little difference with pre layout simulation results.

Table 5. power consumption, post layout simulations, T = 25°C (nW)

VDD(V)	Hold mode	Read mode	Write mode
0.5	0.038	153	0.78
0.4	0.017	34	0.43
0.3	0.0075	2.65	0.058

Table 6. Proposed 7T cell performance parameters, post layout simulations, T = 25℃ (mV)

VDD(V)	HSNM	RSNM	WM
0.5	187	184	144
0.4	140	133	101
0.3	92	88	57

Table 7. Delays for the proposed 7T cell, post layout simulations, T = 25℃ (nS)

VDD(V)	RTD	WTD
0.5	1.65	0.98
0.4	4.43	1.57
0.3	25	4.1

5. CONCLUSIONS

In this paper, a new bit interleaving sub-threshold 7T SRAM cell with different paths and the boosted voltage to read and write word line (VDD + 0.3 V) is presented that improves cell performance compared with conventional 6T SRAM cell. To improve the reading operation, an access buffer is used that separates storage node from read access transistor. Also, to reducing leakage, the virtual ground is used and its control circuits are presented. With techniques used in the cell such as removing driver transistor, suggested 7T cell area is improved against other bit-interleaving cells. On the other hand, combining different techniques and applying multi-Vt transistors in the suggested 7T cell design increase the cell performance similar to other 10T and 12T bit-interleaving cells. The proposed 7T SRAM cell performs effectively write operations with high speed while the cell is without half-select problem. Simulation results in a PTM 32 nm technology show that the proposed design improves power consumption compared with other cells. Furthermore, the proposed cell in comparison with similar SRAM cells, which are compatible with bit interleaving structure has better performance in write and read modes.

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