DESIGN AND ANALYSIS OF PHASE-LOCKED LOOP AND PERFORMANCE PARAMETERS

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ABSTRACT

In this paper, we are present design and analysis of PLL, which is simulated in CMOS 0.18µm technology. The digital phase locked loop achieves locking within about 100 reference clock cycles. The pure digital phase locked loop is attractive because it is less sensitive to noise and operating conditions than its analog counterpart.In this PLL circuit successfully achieved 1.55GHz frequency. Jitter is 1.09ns achieved is very less. Also achieve low phase noise -98.5827 at 1MHz Frequency.

KEYWORDS

PLL, Phase Frequency Detector, Charge Pump, Low Phase Noise, Low Jitter

1. INTRODUCTION

Phase locked loop (PLL) has been widely used in frequency synthesis and data recovery circuits. There is a large design effort and time spent to design a new PLL with different frequencies for different applications. Therefore, a portable digital PLL design is very attractive. Commonly cited weakness of phase-locked loops (PLLs) against delayed-locked loops (DLLs) is jitter accumulation, which refers to the continued increase in the phase error even while the feedback loop is trying to correct it. [1]. Phase Locked Loop is one of extensively used circuits for fast clocks in digital circuits. Predictably PLL was made using analog building block. Using a PLL in a digital noisy System on Chip that affects environmentally complicated integrating and interfacing issues.[2].

The output phase noise of the PLL is usually contributed from the phase noises of the voltage-controlled oscillator (VCO), the phase-frequency detector (PFD), and the input reference signal. In general, the phase noise of the VCO to the output of the PLL is a high-pass response, while the PFD and reference to the output are a low-pass response. To achieve a low-jitter low-phase-noise PLL, the loop bandwidth should be properly designed. However, the phase noise of the VCO degrades as the operation frequency increases toward microwave and MMW bands. Therefore, a wide loop bandwidth can be chosen for suppressing the phase noise of the VCO, but the widest loop bandwidth is usually limited by the input reference frequency due to the consideration of stability. [4]

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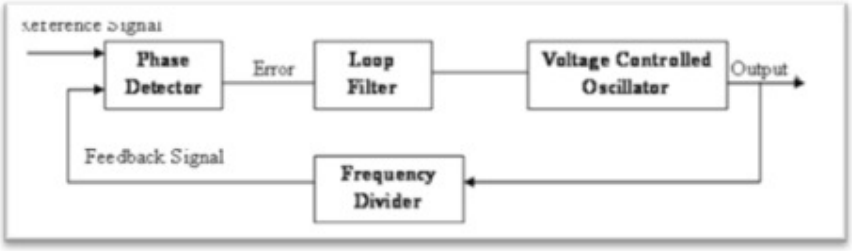

Figure 1:PLL Block Diagram[2]

Figure 1 consists of four blocks i.e. phase detector, loop filter, voltage controlled oscillator and frequency divider.

2. PHASE FREQUENCY DETECTOR

In figure 2 diagram of PFD is shown. O/p of the PFD depends on both phase as well as frequency of the inputs. That type of phase detector is known as sequential detector. PFD is digital circuit which detects phase or frequency difference between reference clock and voltage controlled oscillator (VCO) clock / feedback signal and generates output signal with increasing and decreasing frequency of VCO. At reset input a high signal will force Q low as reset signal is applied. Lastly, a rationally high on both output causes resetting of both FFs. Output signal depends not only on the phase error but correspondingly on frequency error.

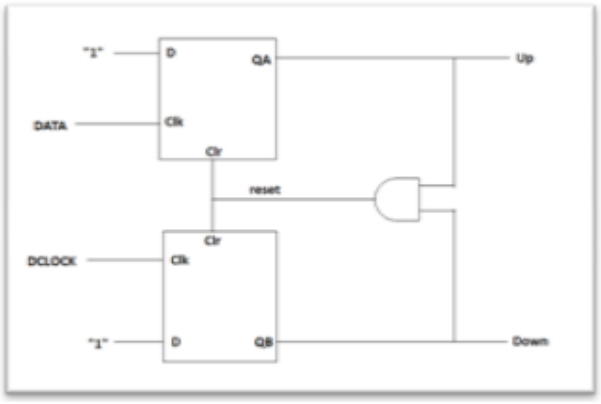

Figure 2: A Basic Block Diagram of Phase Frequency Detector[5]

The implementation of PFD is as shown in figure 3. In the Phase Frequency Detector, the operating frequency is 1 GHz. Means there is higher operating Speed. So, this is the High-Speed Phase Frequency Detector.

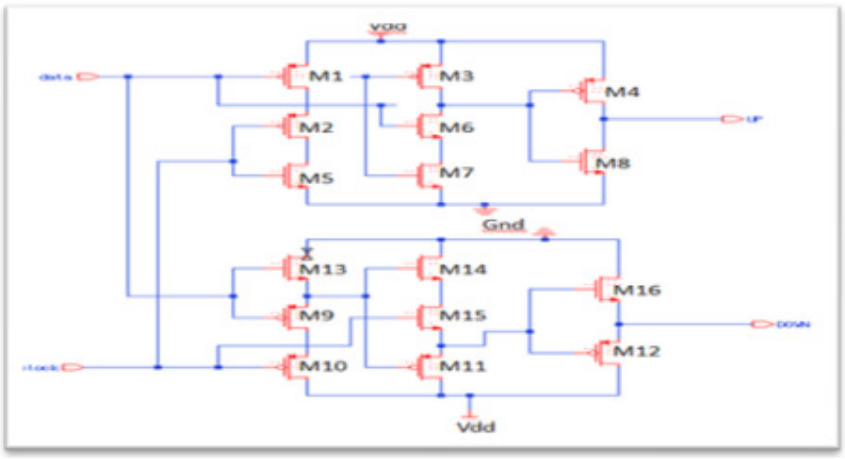

Figure 3: Schematic of Phase Frequency Detector [5]

2.1. Simulation Results in 0.18µm Technology

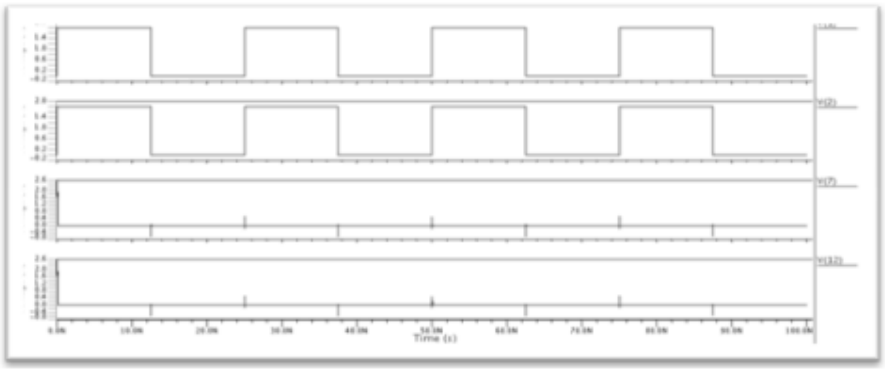

Figure 4: PFD at 50MHz (lock condition)

2.2. Comparative Analysis of PFD

Table 1: Simulation Result in 0.18µm Technology

Parameter	PFD	PFD	PFD
Technology	0.18µm	0.18µm	0.18µm
Input Frequency	50MHz	500MHz	1 GHz
Transistor count	16	16	16
Power Consumption	16.29 nW	33.289 nW	58.714 nW
Dead zone	35ps	32ps	31ps

3. CHARGE PUMP

The next block after the phase frequency detector is Charge pump. Output signals down and up is generated by PFD which is directly connected to charge pump. Main purpose of charge pump is to convert logic states of phase frequency detector into analogy signals suitable to control the VCO [2]. When VCO o/p frequency is same to reference frequency then lock condition of PLL is established. During this period, PFD will deactivate both signals. Hence switches S1 and S2 will

opened till the VCO output frequency changes. Since switches are open, there is no current path formation.

Figure 5 shows general operation of CP can be observed, which describe idyllic behaviour of the charge pump. CP charges or discharges the current of charge pump related to value of error signal generated by PFD.

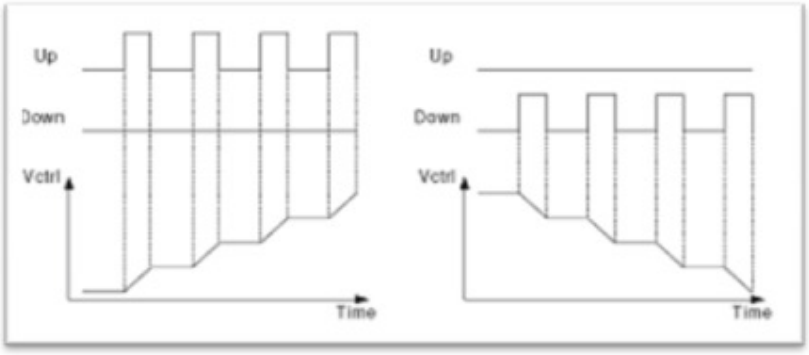

Figure 5: Ideal Behaviour of Charge Pump [2]

This CP circuit is simulated with the 0.18 um CMOS technology as shown in Fig.6. Related to the value of the error signal which is generated by the PFD, it charges or discharges the current of the charge pump.

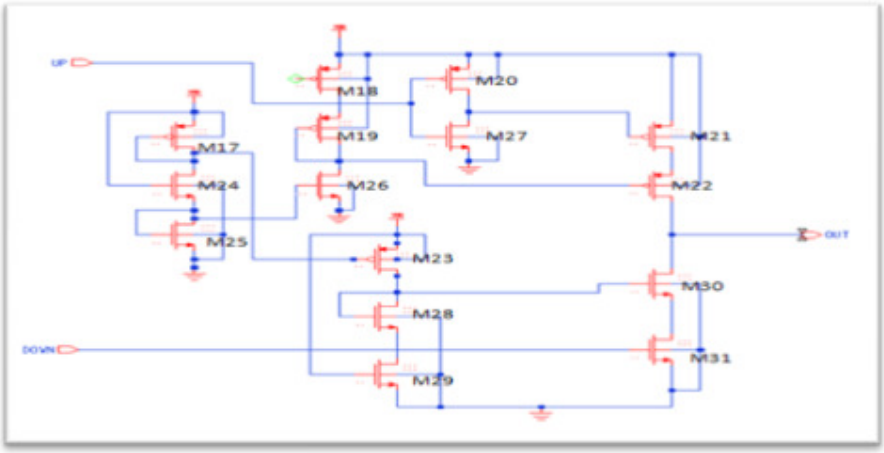

Figure 6: Schematic of Charge Pump Circuit [6]

3.1. Simulation Resultsin 0.18µm Technology

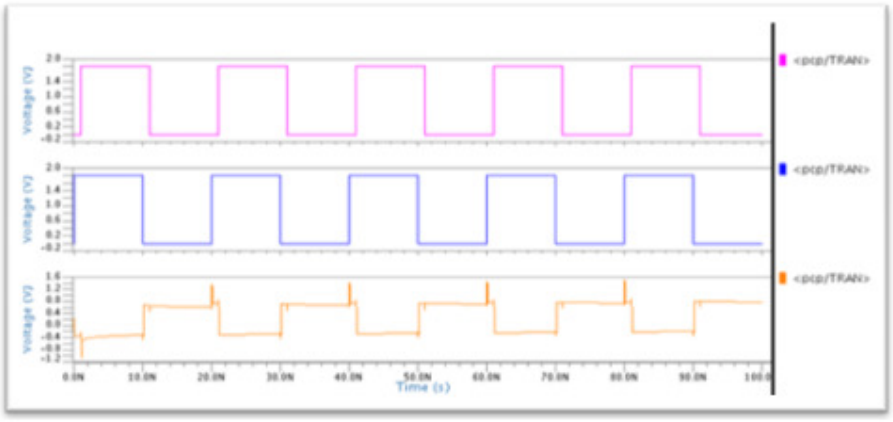

Figure 7: Output Waveform of Charge Pump Circuit

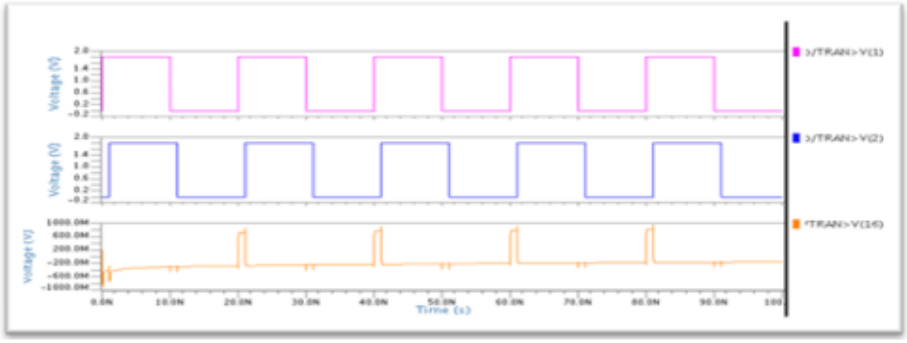

Figure 8: Combine Output Waveform of PFD & Charge Pump Circuit

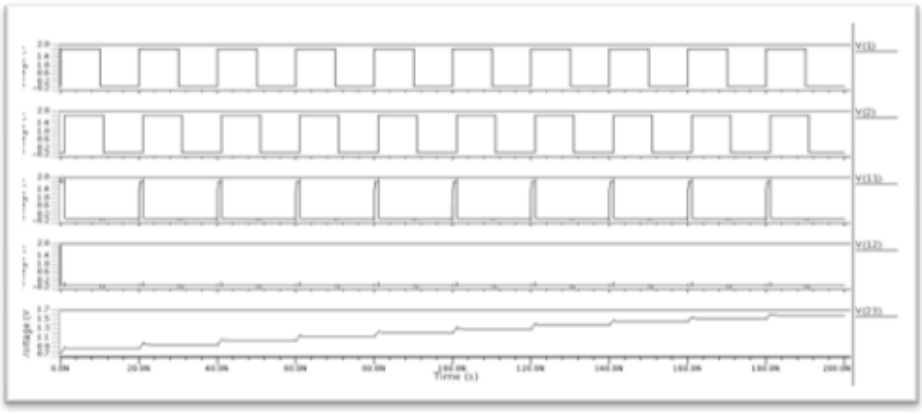

Figure 9: Combine Output Waveform of PFD, Charge Pump & Loop Filter

4. THE CURRENT STARVED VCO

The schematic of Current Starved VCO is shown in Fig. 10. M2 and M3 MOSFETs are operating as inverter, whereas as current sources MOSFETs Ml and M4 operate. Inverter is starved for current is said when the current sources are limit the current available to the inverter. The MOSFETs M5 and M6 drain currents are set by the input control voltage and they are same. At each inverter/current source stage the currents in M5 and M6 are mirrored. Input impedance is an important property of the VCO used in any of the CMOS DPLLs. The filter configurations on the fact that the input resistance of the VCO is practically infinite and the input capacitance is small compared to the capacitances present in the loop filter. Achieving infinite input resistance is usually an easy part of the design. [7]

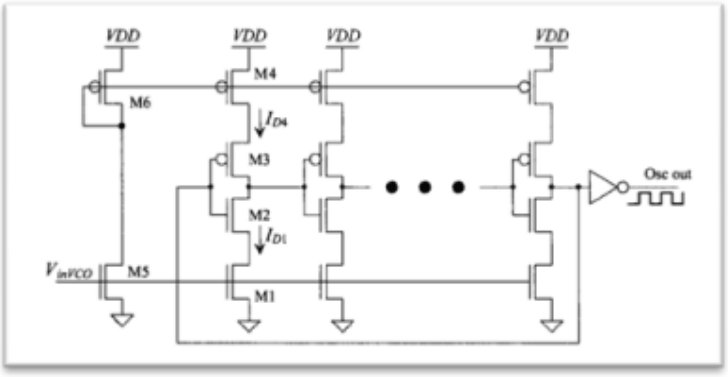

Figure 10: Current-starved VCO [7]

4.1. Simulation Results in 0.18µm Technology

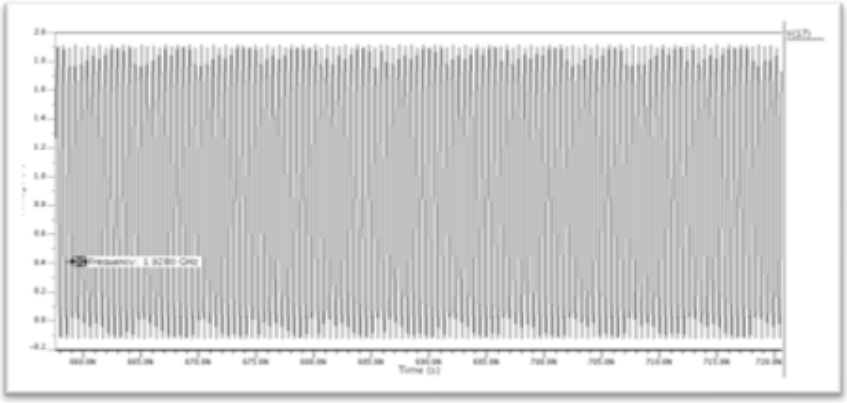

Figure 11: Output Waveform for 1.3v control voltage of CSVCO

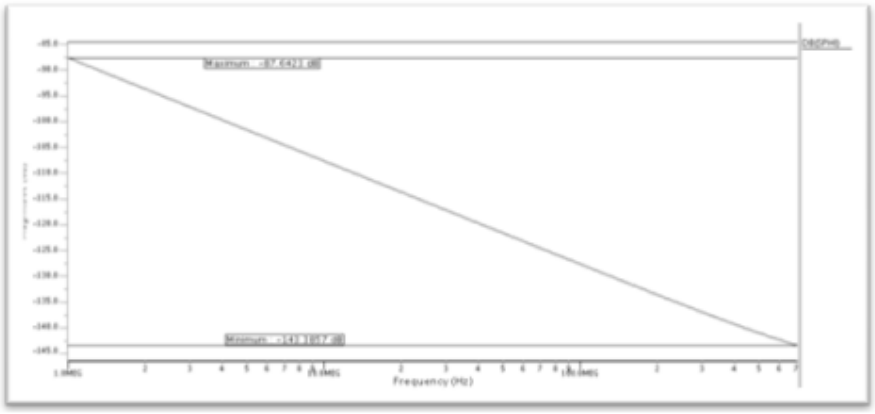

Figure 12: Phase Noise Plot versus offset Frequency CSVCO at 1MHz

Table 2: Simulated Results for Current-Starved VCO

Control Voltage (V)	Oscillating Frequency (MHz)
0.6	129.36
0.7	296.88
0.8	519.38
0.9	1059.7
1.0	1332.7
1.1	1563.2
1.2	1757.8
1.3	1928

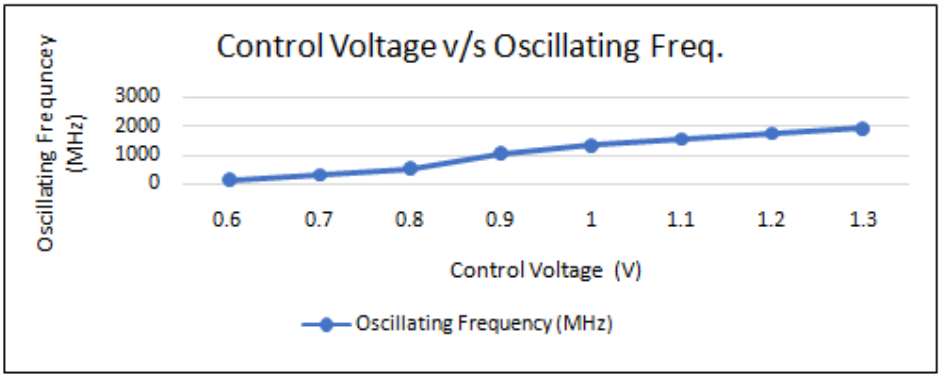

Figure 13: Control Voltage versus Oscillating Frequency Plot for CSVCO

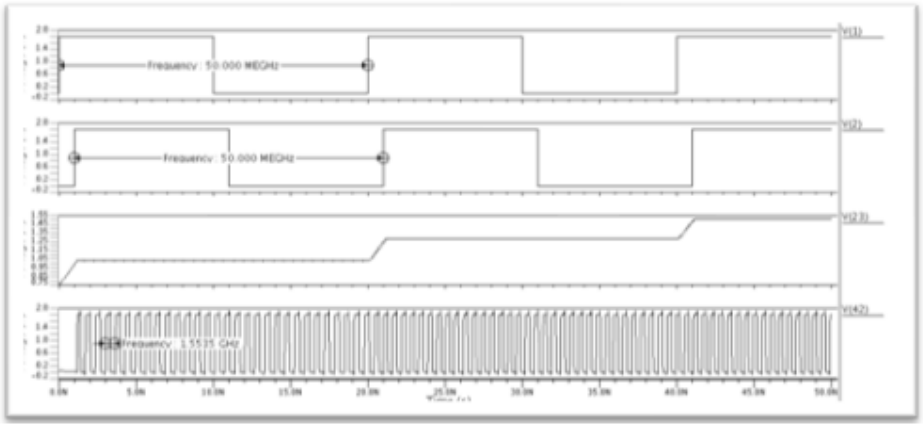

Figure 14: Combine Output Waveform of PFD, Charge Pump, Loop Filter & VCO

5. DIVIDE BY COUNTER

The divider network is feedback given to the phase frequency detector. We can vary the divider network for synthesis of different frequencies. It divides the clock signal of VCO and generate DCLOCK, then applied to phase frequency detector which compare it with input data signal DATA.

The divider network is feedback given to the phase frequency detector. Here divide by 4 counter is used, we can vary the divider network for synthesis of different frequencies. It divides the clock signal of VCO and generate DCLOCK as shown in figure 19, then applied to phase frequency detector which compare it with input data signal DATA.

Here VCO frequency is 1.92 GHz so the output of the divide network becomes approximately 525.77 MHz frequency. In figure 4.56 see the simulation result of divide by 4 counter.

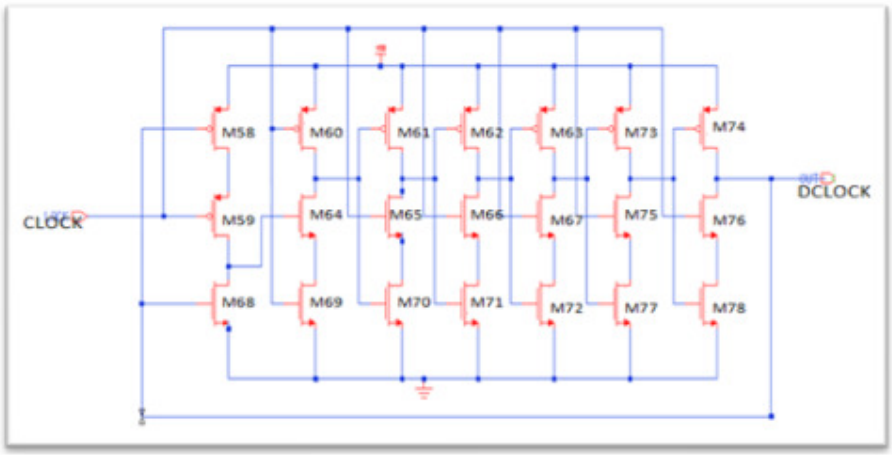

Figure 15: Implementation of Divider Counter by 4

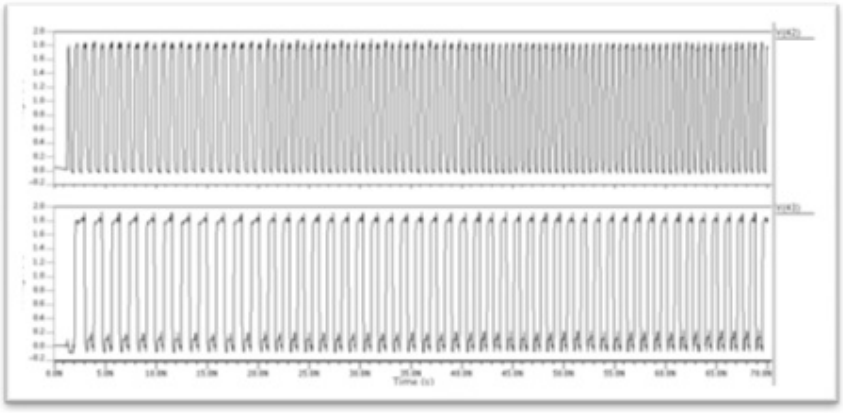

Figure 16: Simulation of Divider Counter by 4

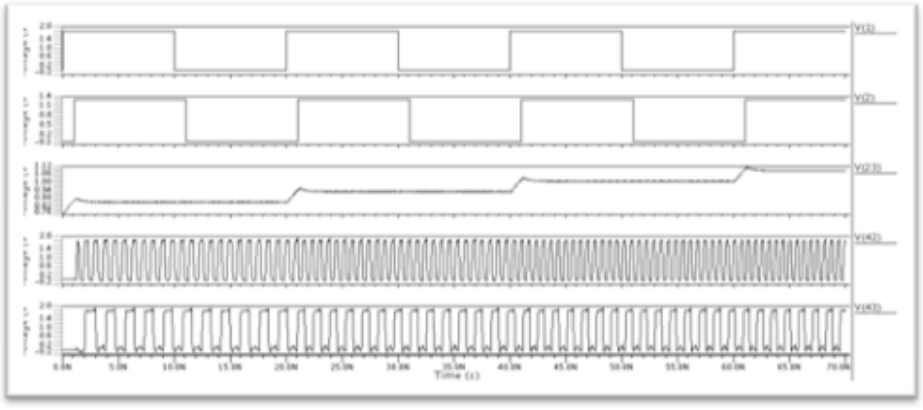

Figure 17: Simulation results of final PLL using 180nm

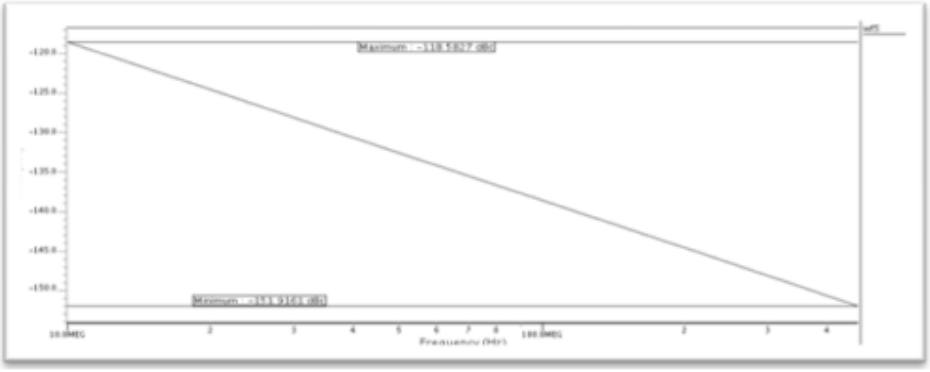

Figure 18: Phase Noise Plot versus offset Frequency of PLL at 1GHz

Table 3: Simulation Results of PLL

Parameter	Digital PLL
Technology	180 nm
Power Supply	1.8 V
Reference Frequency	50 MHz
Centre Frequency	700 MHz
Transistor Count	78
Frequency Tuning Range	1 GHz - 1.55 GHz
Power Consumption	6.92 mW
Phase Noise	-38.5827@1MHz
Jitter	1.09 ns

6. CONCLUSION

This paper is presented a PLL with better designed in CMOS 0.18µm technology. The simulation results allow the circuit designer to fully explore the trade-offs like Dead-Zone, Glitch period and power consumption. The goal of this design is to achieve more than 1GHz and successfully achieved 1.55GHz frequency. Jitter is 1.09ns achieved is very less. Also achieve low phase noise -98.5827 at 1MHz Frequency. RMS transient value is 246.49mV and power consumption is 6.92mW

REFERENCES

[1] Sally Safwat, Amr Lotfy, MagedGhoneima and Yehea Ismail, "A 5-10GHz Low Power BangBang All Digital PLL Based on Programmable Digital Loop Filter", 2012 IEEE

[2] Raj Nandini, Himadri Singh Raghav, B.P.Singh, "Comparison of Phase Frequency Detectors By Different Logic Gates", International Journal of Innovative Technology and Exploring Engineering (IJITEE) ISSN: 2278-3075, Volume-2, Issue-5, April 2013.

[3] Ronald E. Best, "Phase-Locked Loops – Design, Simulation and application", 5th edition, TATA McGraw-Hill

[4] Hong-Yeh Chang, Yen-Liang Yeh, Yu- Cheng Li u, Meng-Han Li, and Kevin Chen, "A Low-Jitter Low-Phase-Noise 10-GHzSub-Harmonically Injection-Locked PLL WithSelf-Aligned DLL in 65-nm CMOS Technology", 2014 IEEE

[5] Jyoti Gupta, AnkurSangal and HemlataVerma, "High Speed CMOS Charge Pump Circuit for PLL Applications Using 90nm CMOS Technology", Middle-East Journal of Scientific Research 12 (11): 1584-1590, ISSN 1990-9233, IDOSI Publications, 2012.

[6] Neelima, Dr. Sandeep K. Arya, Manoj Kumar,"A Study on Various Voltage Controlled Ring Oscillators in 0.35µm and 0.5µm Technologies".

[7] R.Jacob Baker, Harry W.Li, David E. Boyee, "CMOS Circuit Design, Layout and Simulation ", IEEE Press Series on Microelectronic System, pp 383-391.

[8] BehzadRazavi, Member, IEEE, "A Study of Phase Noise in CMOS Oscillators", IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 31, NO. 3- MARCH 1996.