A 2.4 GHz Fully Integrated LC VCO Design Using 130 nm CMOS Technology

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ABSTRACT

In this paper, a 2.4 GHz fully integrated LC voltage controlled oscillator (VCO) for RF wireless applications is presented. The VCO circuit is designed using TSMC 130 nm CMOS process. The circuit design is based on differential oscillator structure with cross-coupled NMOS transistors which achieves low power dissipation and low phase noise. Simulation and layout of the VCO is carried out using ADS Tool. The VCO operates from a supply voltage of 1.8 V and consumes 19.62 mW of power. After simulating the proposed design the VCO shows a phase noise of -128.68 dBc/Hz at 1 MHz offset frequency from a 2.4 GHz carrier signal. The frequency range of the VCO is from 2.36 GHz to 2.61 GHz when the control voltage changes from 0 to 2 V. The FOM is obtained as -183.73 dBc/Hz. The total chip area, including pads, occupies 0.7 mm × 0.7 mm.

KEYWORDS

VCO, CMOS process, NMOS cross-coupled, phase noise, ADS (Advanced Design System), FOM (Figure of Merit)

1. INTRODUCTION

With the tremendous growth of wireless communication technologies there is a continuous demand for low cost, low power and high integration on-chip solutions in the RF wireless industry. Such higher integrations will be feasible only with the progress of VLSI industry which permits the MOSFETs to be used for low-noise RF applications. The VCO being an important component in the radio transceiver, its design is an attractive topic for the continued research and still is an active research area. VCO plays a vital role in many applications such as GSM, Bluetooth, WLAN, Wireless Personal Area Network (WPAN) and Wireless Sensor Network etc. [1].

For the microwave monolithic integrated circuit (MMIC) VCO designs, the general specifications are phase noise, tuning range and power consumption. As the operating frequency for such MMIC designs is as high as several hundred GHz, low power consumption and low phase noise are the major concerns. At a given power consumption, LC oscillators have a much higher frequency stability and spectral purity since it is set by the passive resonator. LC oscillators are widely used for RF transceivers, because of its easier implementation and low phase noise performance [2]. In the last few years many integrated LC VCOs have been implemented in CMOS technology and emerged as a critical component in design of most of the RF systems [3]-[5]. To achieve the low phase noise, low power and low cost, on-chip VCO with no external components is the best choice.

This paper is organized as follows. Section 2 describes the design of VCO circuit. Section 3 and Section 4 presents the simulations results and layout of the VCO as well as discussions. Finally, Section 5 and Section 6 summarizes and concludes the results.

2. VCO CIRCUIT DESIGN
2.1. VCO Circuit Schematic

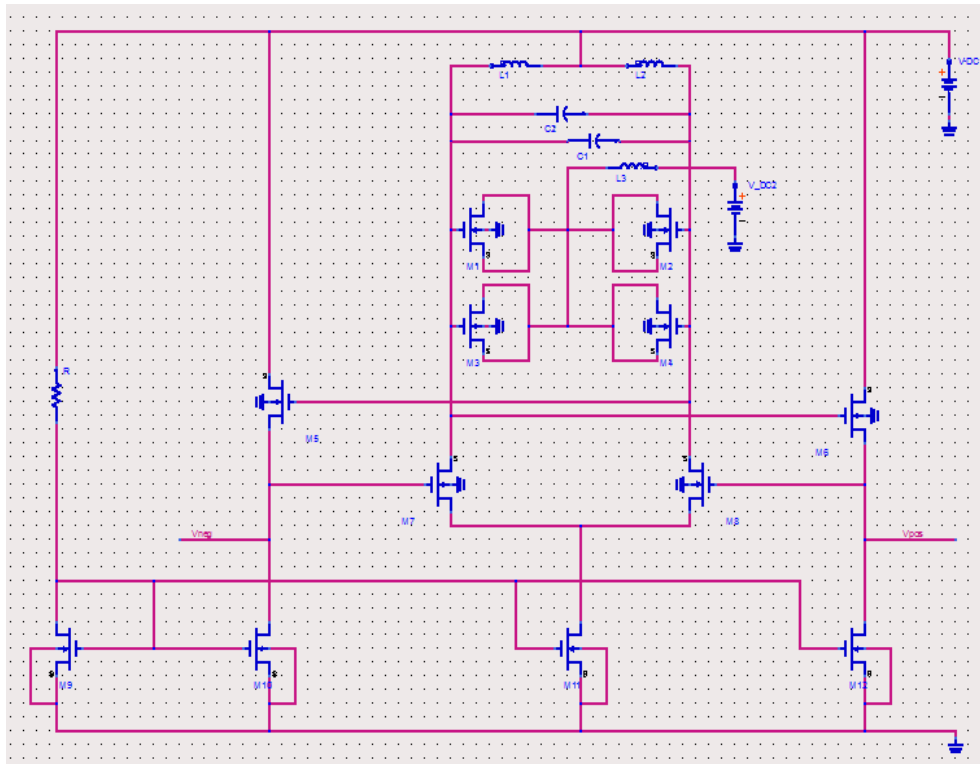The implemented design uses a NMOS cross-coupled structure as shown in Figure 1.

Figure 1. Schematic of NMOS Cross-coupled VCO

The NMOS cross-coupled topology has been chosen because it shows the higher transconductance per unit area, and hence smaller transistor capacitances will contribute to the total parasitic capacitance of the resonant tank circuit. Also it gives the best overall performance in terms output voltage swing, bias current, phase noise, power dissipation, and total chip area required. To tune the output frequency of the VCO, a varactor circuit implemented with the help of four transistors structure as shown in Figure 1, is applied to vary the capacitance. The varactors are implemented with the help of MOSFETs by shorting its drain and source terminals and applying voltage between its gate and the short terminal.

The VCO can be made oscillating more easily by increasing the fingers of MOSFETs but this will lead to a bigger parasitic capacitance. The fixed capacitance, a varactor capacitance provided by four transistor structure and the parasitic capacitance gives the total capacitance of the circuit. To make sure a wide output frequency range, the tuning range of varactors Cmax/Cmin (maximum capacitance/minimum capacitance) should be as large as possible. The effect of adding a fixed capacitance in parallel with the LC tank is such that it adjusts the resonance frequency of the tank circuit and lowers the gain of the varactor.

2.2. Oscillation Start-up Condition

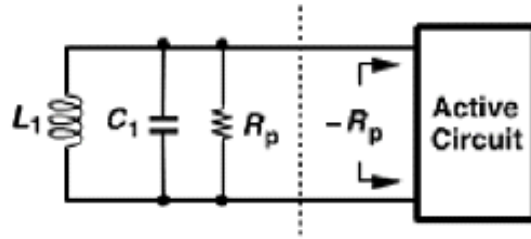The LC VCO can be viewed as a negative resistance oscillator.

Figure 2. A Practical LC Tank Circuit

In an ideal LC resonator circuit, the energy in the form of the magnetic and electric energy, transfers back and forth between the inductor and the capacitor without any loss of power. However, the parasitic resistances associated with L and C leads to a practical parallel RLC circuit as shown in Figure 2. Due to the energy loss associated with the resistor, the oscillating signal is damped over time while exchanging the energies between L and C. So an active circuit is needed that provides the negative resistance which cancel out the positive loss of the tank in order to maintain the undamped oscillation.

This negative resistance ─ Rp is the resistance provided by the cross-coupled NMOS transistor pair and it can be expressed as

$$Rp = -\frac{2}{gm} \tag{1}$$

where, gm is the transconductance of the NMOS transistors in the cross-coupled pair and factor of 2 accounts for the differential NMOS structure.

In practical LC tank circuit, the negative resistor -Rp must cancel the loss associated with LC resonator. The start-up condition to initiate oscillation is

$$Rp \geq -\frac{2}{gm} \tag{2}$$

Equation (2) can be expressed as

$$gm \geq -\frac{2}{Rp} \tag{3}$$

For the LC resonator, we have Rp=L/CR. Where R is the equivalent series loss associated with the tank. Equation (3) becomes

$$gm \geq \frac{2CR}{L} \tag{4}$$

To ascertain a stable frequency of oscillation the value of capacitor and inductor should be small and large respectively.

The resonant frequency of the oscillator can be approximately expressed as

$$fo = \frac{1}{2\pi\sqrt{LC}} \tag{5}$$

2.3. Phase Noise

Phase noise gives the measure of the spectral purity of the VCOs output signal. Phase noise is a critical and important parameter in RF wireless design. Phase noise of the VCO can be expressed as [6]

$$L(\Delta f) = 10 log \left\{ \left[1 + \left(\frac{f_0}{2\Delta f Q} \right)^2 \right] \left(1 + \frac{f_c}{\Delta f} \right) \frac{FkT}{2P_{av}} + \frac{2kTRK_{vco}^2}{\Delta f^2} \right\} \tag{6}$$

where, $L\{\Delta f\}$ is the phase noise at the frequency offset Δf from the carrier signal at f_o, f_o is the carrier signal frequency in Hz, Q is the quality factor of the tank circuit, F is the noise factor, T is the temperature in Kelvin, k is the Boltzmann's constant in J/K, R is the equivalent noise resistance of the varactor, P_{av} is the oscillator output average power, K_{vco} is the voltage gain of the VCO in Hz/V.

3. SIMULATION RESULTS

This VCO is designed using the TSMC 130 nm CMOS process technology and simulations are carried out using the Advanced Design System (ADS) produced by the Keysight Technologies Inc. The Keysight Technologies, Inc. ADS is the world's leading electronic design automation (EDA) software for RF, microwave, and high speed digital applications. ADS offers a solution that combines schematic, layout, circuit and technologies for IC and packaging in a single-vendor, integrated platform solution. ADS provides the most complete set of advanced simulation tools, seamlessly integrated into a single environment, that flows from schematic entry to tape-out and packaging. These tools enable to verify, prior to fabrication, that the RFIC/MMIC design meets all specifications in its final package. Various simulations such as S-parameter linear frequency-domain simulation, harmonic balance nonlinear frequency domain simulation, transient/convolution time-domain simulation are can be carried out using ADS. ADS also supports DRC/LVS, a full-featured tool for generating production ready RF layouts. With the use of ADS tool the measurement results are generally found to be well consistent with the simulated results except the small variations in the phase noise and carrier frequency which are caused due to the process variation in fabrication.

The VCO operates from a supply voltage of 1.8V and has a total DC power consumption of 19.62 mW including the buffer circuit.
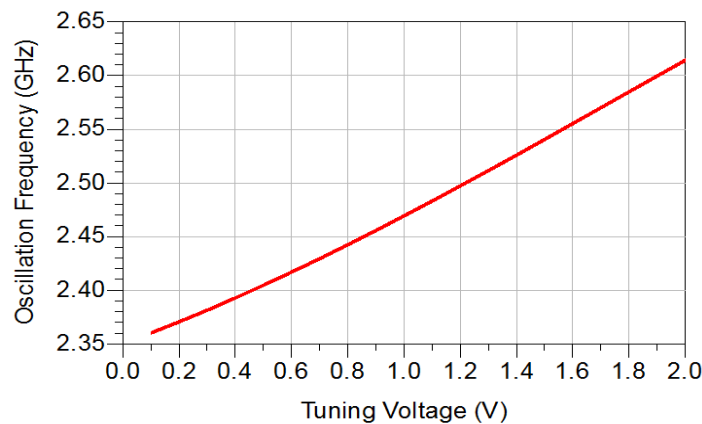

Figure 3. Tuning Range of VCO

When the control voltage changes from 0 to 2 V, the frequency of VCO varies from 2.36 GHz to 2.61 GHz, which corresponds to tuning range of 250 MHz. Thus the VCO gain, KVCO, can be calculated as 125 MHz/V. The tuning range of the VCO is shown Figure 3.

The simulated phase noise performance of the VCO is shown in Figure 4. It can be seen that the VCO has a phase noise of -128.68 dBc/Hz at 1 MHz offset frequency from a 2.4 GHz carrier signal. As the KVCO is relatively high, the phase noise performance can be further improved without sacrificing the tuning range, by reducing the gain of the varactors which reduces the KVCO.
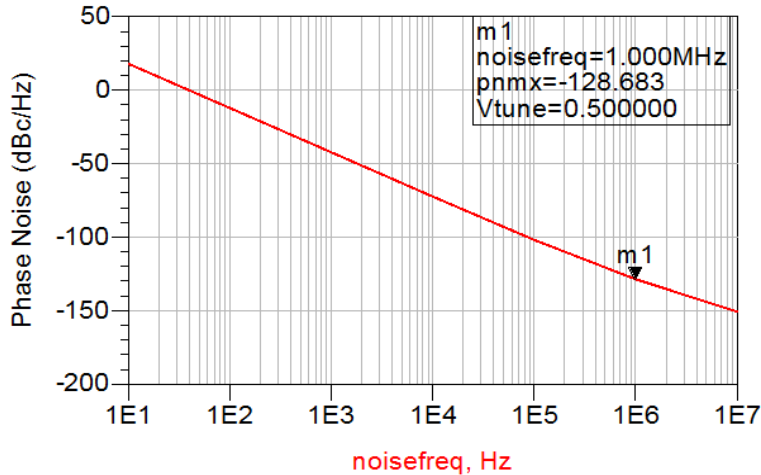

Figure 4. Phase Noise of VCO at 1 MHz Offset

The transient output response of the VCO is shown in Figure 5. A transient simulation is a relatively fast way to verify the functionality of the VCO and estimate its settling time and output frequency.
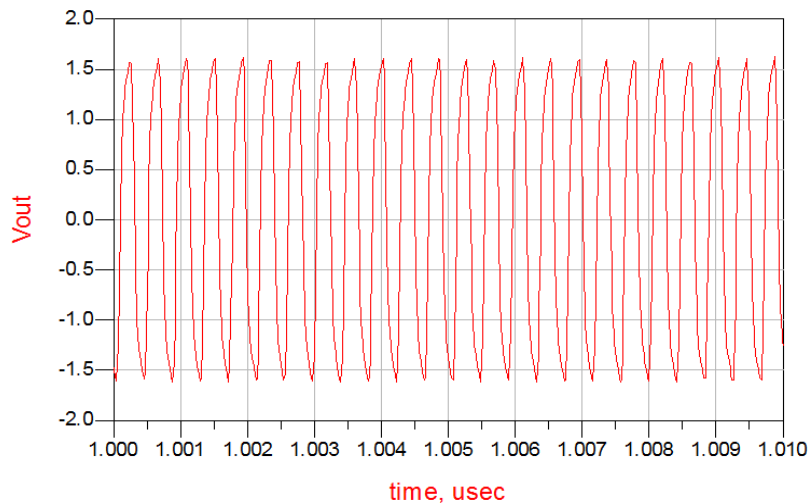

Figure 5. Transient Output of VCO

The circuit generates stable periodic oscillations with harmonic index as shown in Figure 6. Harmonic balance simulation, simulates the circuit with multiple input frequencies and calculates the steady state response of the circuit.
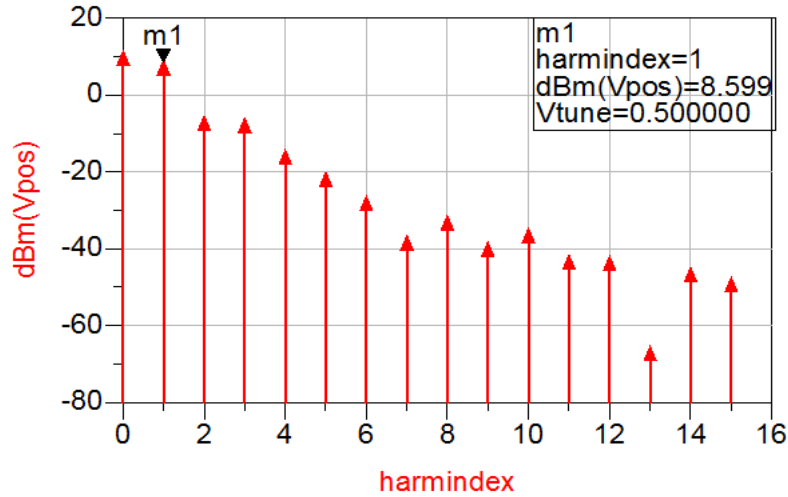
Figure 6. Harmonic Index of VCO

Due to the differential output voltage of the NMOS cross-coupled transistors, the VCO generates two out of phase signals at its output. Figure 7 and Figure 8 shows the output signals of the VCO at the positive and negative output nodes respectively.
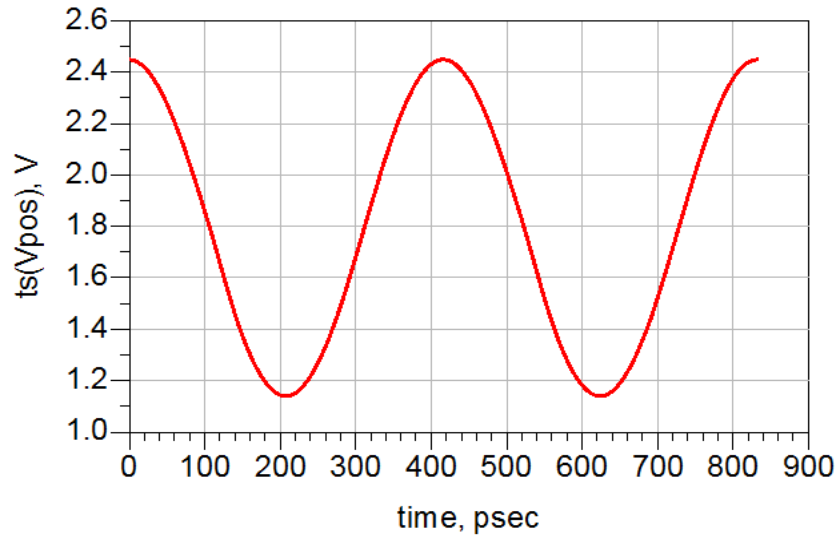
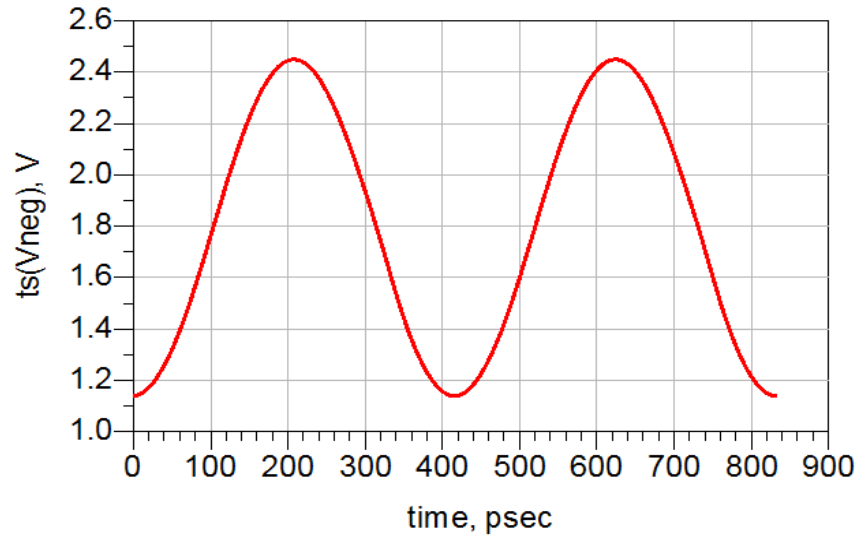

Figure 7. Vo+ Output Signal of VCO

Figure 8. Vo- Output Signal of VCO

4. LAYOUT DESIGN
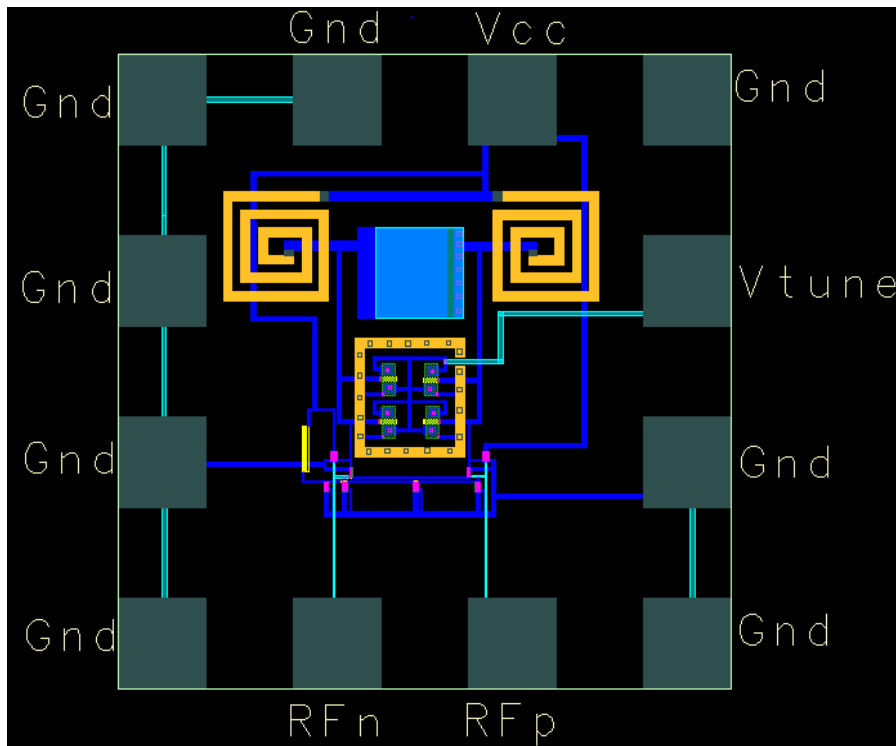
The layout of this LC VCO is shown in Figure 9.

Figure 9. Layout of the VCO

The "RFp" and "RFn" are the differential output nodes of the LC VCO. The "Vtune" is the port for controlling the tuning voltage of the oscillator. While designing the layout, the LC tank should be placed as symmetry as possible, which makes the two output nodes to have equivalent

output impedance. An imbalance will result if there is any asymmetry in the two sides of the oscillator tank causing the center frequency to change. One important design consideration during the layout of the VCO is its metal width. The resonating tank causes the current in the tank to be Q times larger. Hence the metal lines connecting the tank components need to be sufficiently large to withstand the large currents [7].

All these factors have been taken into account while making the layout of this VCO. Including all the pads, the total chip area of the VCO occupies 0.7 mm × 0.7 mm, where the VCO core area occupies only 0.43 mm × 0.36 mm. The measurements of VCO IC are carried out using the ADS layout tool.

5. FIGURE OF MERIT

To compare the performance of the VCO with previously published literature a widely used figure of merit (FOM) parameter can be stated by Equation (7) as

$$FOM = L\{\Delta f\} - 20\log\left(\frac{f_o}{\Delta f}\right) + 10\log\left(\frac{Pd_c}{1mW}\right) \tag{7}$$

where, the figure of merit in dBc/Hz, Pdc is the power consumption in mW and L{Δf} is the phase noise at the frequency offset Δf from the carrier signal at fo. The FOM of the VCO is calculated to be -183.73 dBc/Hz at the centre frequency of 2.4 GHz and for a power dissipation of 18mW.

Table 1 gives a brief description of the performance comparison of the proposed VCO with the previously published works. It can be determined from Table 1 that our design shows superior phase noise performance when compared with previous works but at the cost of power consumption.

Table 1. Performance Comparison of VCO with Previous Works

Parameters	This work	[3]	[4]	[5]
Technology (nm)	130	180	130	180
Supply Voltage (V)	1.8	0.25-0.5	1.2	1.8
Power Dissipation (mW)	19.62	2.82	0.5	3.8
Tuning Range (MHz)	250	260	40	4000
Frequency (GHz)	2.4	2.29	0.4	5.5
Phase Noise (dBc/Hz)	-128.63 @1M	-118.9 @1M	-138.00 @1M	-95.6 @1M
FOM (dBc/Hz)	-183.73	-181.6	-193.05	-164.90

6. CONCLUSION

The design of a fully integrated 2.4 GHz low phase noise LC VCO implemented using TSMC 130 nm CMOS technology is presented. VCO design is based on differential oscillator structure with cross-coupled NMOS transistors. The VCO operates from a supply voltage of 1.8V and has a total DC power consumption of 19.62 mW including the buffer circuit. The VCO simulations and layout are carried out using ADS Tool. The simulated phase noise of the VCO is found to be -128.68 dBc/Hz at 1 MHz offset from the carrier frequency at 2.4 GHz. The linear tuning range of this VCO is observed to be ranging from 2.36 GHz to 2.61 GHz when the tuning voltage is varried from 0 to 2 V, corresponding to a 10% tuning range. The FOM value is calculated to be -183.73 dBc/Hz. The total chip area of the VCO IC including the pads is found to be 0.7×0.7 mm2. The future scope of this work includes fabrication of the designed VCO chip and its physical testing and thereafter comparing the simulated and the measured performance of the design. This design finds its applications in RF wireless communication applications because it offers low power, high performance (low phase noise), wide tuning range and small size (low cost).

ACKNOWLEDGEMENTS

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