ONE BIT 8T FULL ADDER CIRCUIT USING 3T XOR GATE AND ONE MULTIPLEXER

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ABSTRACT

This paper is present very common arithmetic circuit .This circuit is faster has low power consumption by using a new 3 transistor XOR gate. It has two basic features high speed & low power consumption .For the arithmetic circuit very useful parameter low power consumption & time delay. The area of a circuit is directly related to number of gates used in a circuit. In the present design one bit 8T full adder minimizes area, and hence power efficiency. This paper contributes to better understanding of the behavior of single bit full adder cell .When low power delay products are essential full adder cell have been implemented in Tanner 14 Ver. suit and simulation using 70nm CMOS technology to obtain of the performance of the cell with respect to time and power consumption.

KEYWORDS

Full adder, MOS, multiplexer, power consumption, PDP, time delay & 70nm technology.

1. INTRODUCTION

Arithmetic function is very common function for the various electronics fields. In many cases determine speed factor for the addition of the numbers. The addition is the very common operation in the electronics circuits. Just like microprocessor, digital signal processing & data-processing application-specific integrated circuits. Minimum time delay & minimum power consumption is the must for the VLSI circuits. Minimum time delay & area is directly depends on the number of transistors. In this paper introduce 8T full adder circuit it's also having minimum no. of transistor that the reason time delay & area is also minimum. In full adder fast carry generation is important factor .For the high speed carry generation can be minimized the worst path delay.

2. PREVIOUS WORK

A survey of literature shows a broad spectrum of different types of full adder that have been actualized over in the last years. The early designs of full adder circuit were based on the 3T XOR gate [2].

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In the last ten years the design of fourteen transistor full adder has been considerable used .It is produced by two XNOR gates & carry by four transistor (MUX).The base of MUX is pass transistor logic. By the two transistor multiplexers based on pass transistor logic it can be reduce the total number of transistor count of adder .By using 12 transistor full adder circuit based on pass transistor logic shows poor noise margin. This paper is introducing 8T full adder circuit .This design is having only two stages. First stage for the sum is having 6 transistors and another stage for the carry is the based on the two transistors multiplexer. The idea is successful for the minimizing delay & high speed of the full adder circuit [1].

3. DESIGN OF THE THREE TRANSISTOR XOR GATE.

The is a 3T XOR gate.

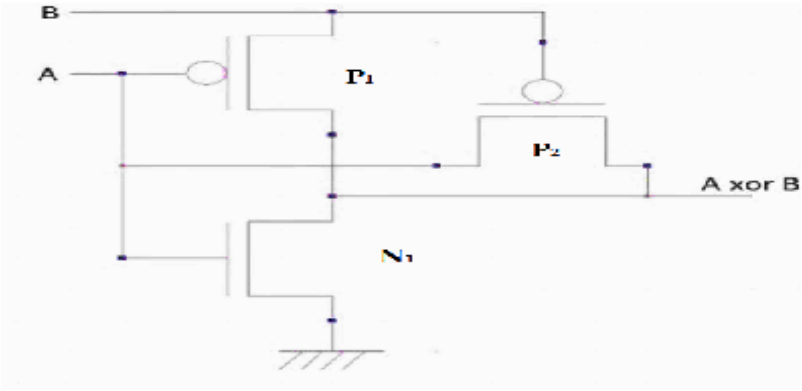

Figure1. 3T XOR Gate

Table1. Truth Table for 3T XOR gate.

A (input)	B (input)	Output
0	0	0
0	1	1
1	0	1
1	1	0

3 transistor XOR gate using in this 8T full adder circuit. This a combination of CMOS inverter & one pass transistor .By this full adder circuit minimizing delay of circuit & power consumption .The XOR gate is based on CMOS inverter and one pass transistor when input B=1the output become of XOR gate is the complement of input A. Another condition B=0 CMOS inverter output goes to high impedance. The pass transistor is switched on and output is same as the A input .The function is like that 2 input XOR gate, when A=1 & B=0. Both the transistor $PMOS_2$ & NMOS trying to switched on because of the W/L ratio $PMOS_2$ threshold voltage is minimum comparative NMOS that the reason PMOS2 is conducted first & the output is same as the A input

.The minimize threshold voltage by increasing W/L ratio of transistor is relates by channel length & width (1).

$$V_T = V_{TO} + \Upsilon\left(\sqrt{V_{SB}} + \phi_0\right) - \alpha_1 \frac{t_{ox}}{L}\left(V_{SB} + \phi_0\right) - \alpha_V \frac{t_{ox}}{L} V_{ds} + \alpha_w \frac{t_{ox}}{W}\left(V_{SB} + \phi_O\right) \quad \text{..... (1)}$$

Where

V_{TO} = zero bias threshold voltage
γ = bulk threshold coefficient
ϕ_f = Fermi potential
t_{ox} = thickness of the oxide layer
α_1 , α_v and α_w = are process dependent parameters

According to this equation (1) by increasing width can be minimized threshold voltage.
A problem is when A=1, B=0 in this condition N_1 transistor region since its gate has a logic high input P_2 transistor is also in active region its gate input voltage is logic low .This difficulty can be overcome by decreasing the W/L ratio.

4. DESIGN OF THE 2×1 MUX

Let us explain 2 input lines having signals as I_0 and I_1 for selecting one of the 2 inputs signals .We require addresses which can be a one bit word the address line are designated as a S_1 .

Table 2. Truth Table for 2×1 Multiplexer

S_1	*OUTPUT*
0	I_0
1	I_1

This truth table can be expressed by the following Boolean expression.

$$\text{Output} = \overline{S_1}\ I_0 + S_1\ I_1 \quad \text{.....(2)}$$

Multiplexer circuit also works as select line $A \oplus B$. $A \oplus B$ =0 the PMOS transistor is activated and its pass A input voltage at output terminal. $A \oplus B$ =1 NMOS transistor is activated is transfer C input voltage at the output terminal. NMOS W/L ratio is 1/1 and PMOS W/L ratio 2/1. MUX output is satisfied full adder carry output. 2×1 Multiplexer shown in fig 2.

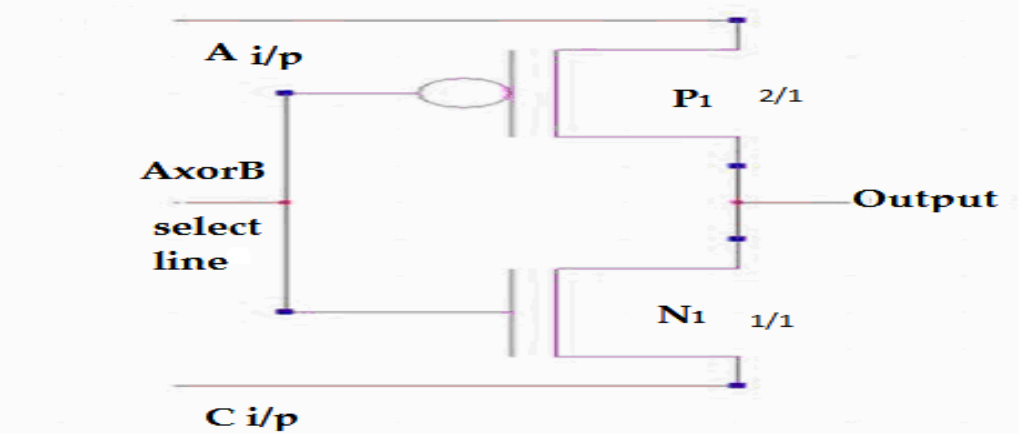

Figure 2. 2×1 multiplexer

5 DESIGN & IMPLEMENTATION OF FULL ADDER CIRCUIT

This present approach as shown in symbolic circuit diagram of figure 3. We have used two XOR cells and transmission gate multiplexer to design the full adder. Sum is generated by two XOR gates Carry output is generated by 2×1 multiplexer (MUX).

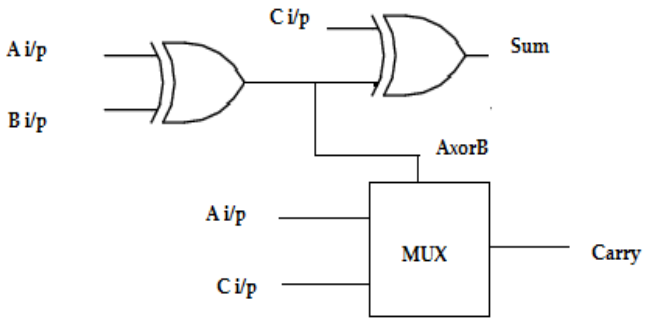

Figure 3. Symbolic Circuit Diagram of full adder circuit

In Schematic circuit diagram of figure 4. Two transistors multiplexer based on pass transistor logic can also be used to generated Carry output which reduces the total transistor Carry output of the adder.

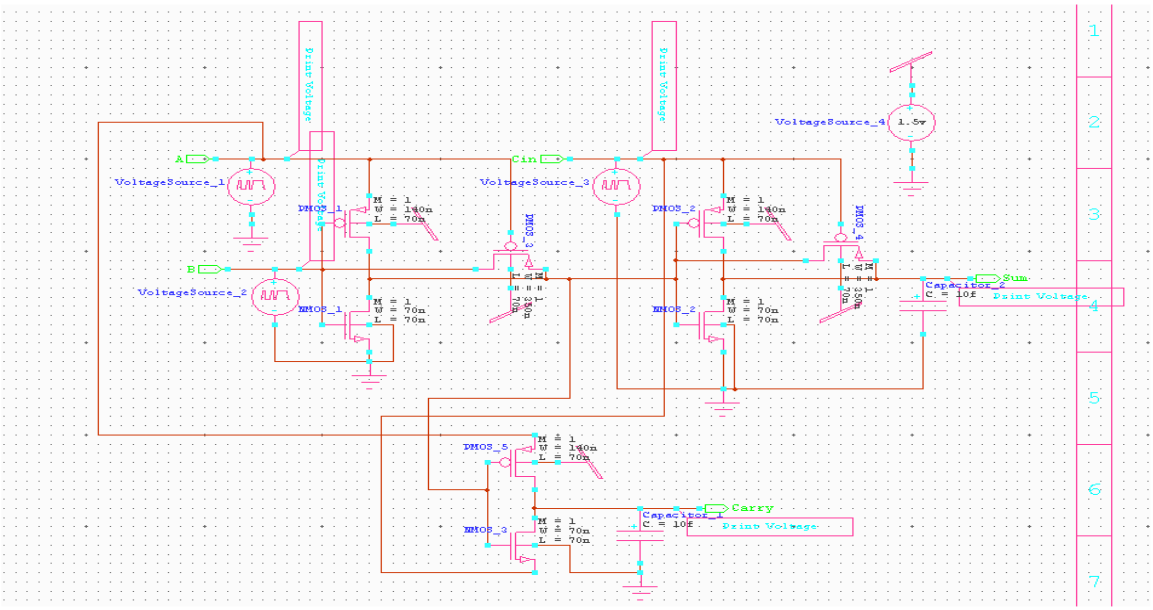

Figure 4. Schematic Diagram of 8T Full Adder.

In single bit full adder circuit is having two XOR gates and one multiplex gate**.** A and B input is connected to the first XOR gate. C input is connected to second XOR gate .A⊕B is select line for MUX, if A⊕B=0 PMOS transistor is selected. A⊕B=1 NMOS transistor is selected. PMOS source terminal is connected to A input voltage and NMOS source terminal is connected to C input voltage.

This design is based on a modified version of a CMOS inverter and a PMOS pass transistor. The input B become a high .The CMOS inverter behaves like a simple inverter .The output become of XOR gate is the complement of input A.

5.1 In case A=0, B=0 and C=0

The B=0 CMOS inverter output goes to high impedance. However the pass transistor $PMOS_3$ is and the output gets the same logic value as the A input. $A \oplus B = 0$ and C=0 in a second XOR gate. When $A \oplus B = 0$ the CMOS inverter output is at high impedance, the pass transistor $PMOS_4$ is enabled and the output get the zero. $A \oplus B = 0$ The $PMOS_5$ transistor is activated its pass A input voltage at the output. The carry output is zero. The operation of the whole circuit is thus like a full adder.

6. SIMULATION AND PERFORMANCE ANALYSIS OF 8T FULL ADDER CIRCUIT

Tanner 14 used as simulation tool finding proposed full adder circuit results .This paper is based on full adder circuit results .This paper is based on 70nm technology the output result is shown in fig 4.

The result of present full adder circuit using By S-Edit calculates by this power, time delay & PDP. By considering the simulation result average power for sum $2.0131e^{-008}$ and for carry $1.8110e^{-010}$ .The average power consumption across to a circuit is 0.499µw. Which is about by using these values we have change in schematic capacitor values has $C_1 = 1ff$, $V_{dd} = 1.2v$ .Since a circuit responds differently to different input combinations. The input output waveforms for the eight transistor full adder are shown in fig 5.

The load capacitance is increase of CMOS full adder circuit. The propagation delay and power dissipation is also increase. The increase width of NMOS transistor, decreasing linearly propagation delay and power dissipation. Power dissipation (P_d) will decrease by decreasing supply voltage (i.e. P_d is proportional to the square of the V_{DD}) .In case of propagation delay (t_p) is inversely proportional to the supply voltage.

Power consumption is calculated by across to the voltage source A, B & C input terminals. And find average power consumption of this circuit shown by fig.5.

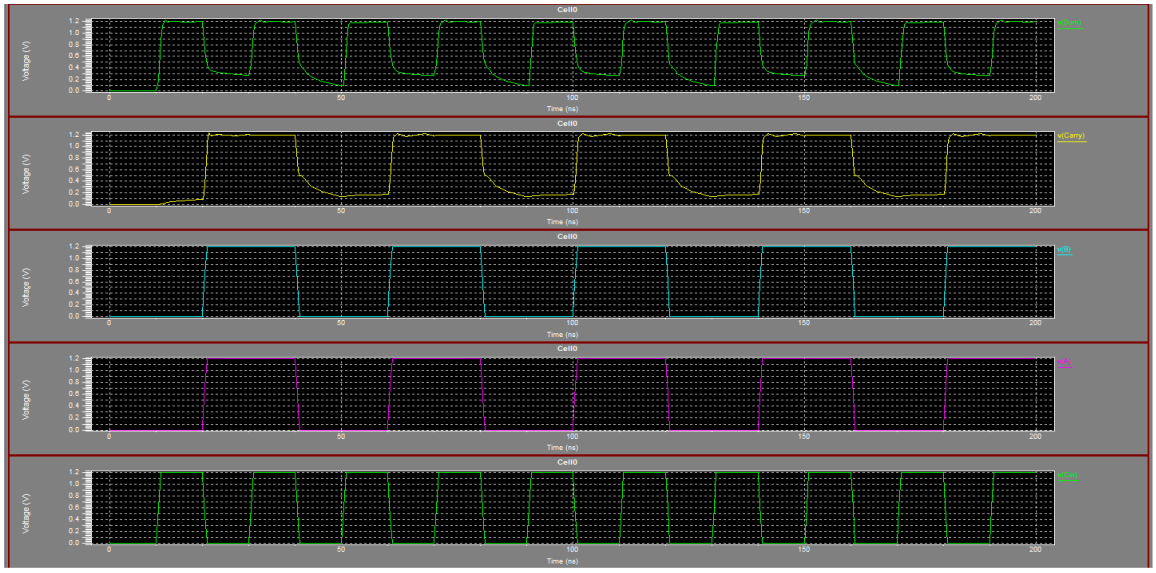

Figure 5.Wave form of 8T full adder circuit.

The width of PMOS is directly proportional to the power dissipation, propagation delay & load capacitor. The supply voltage, width of NMOS, PMOS loads capacitor all this parameter value is minimum that the reason power dissipation is also minimum. The power –delay –product (PDP) is important parameter for VLSI circuits .This is the product of time delay & power.

Table 2. Performance Table of Full Adder Circuits

Design	Technology	No. of Transistor	Power Consumption	Time Delay	PDP
Proposed	70nm	8T	0.499µw	10.15ns	5.065fj
[9]	90nm	8T	87.53 µw	33ps	2.89fj
[6]	90nm	14T	8.85 µw	125.8ps	1.113fj
[8]	180nm	9T	4.065 µw	21.91ps	0.089fj
[2]	350nm	14T	132 µw	160ps	21.12fj

The above table gives comparative analysis of performance of different full adder circuits. The proposed 8T full adder circuit is better than technology of 90nm, 180nm, and 350nm. There is only one drawback in the proposed circuit that it has poor time delay comparative other circuits.

7. CONCLUSION

A new design for full adder is proposed and single bit full adder based on 3T XOR gate using 8 transistors has been designed .Proposed adder shows power consumption of 0.499µw maximum output delay 10.15ns and PDP is 5.065fj with supply voltage of 1.2 v .Adder has been compared with earlier reported with reduced transistor Carry output than earlier reported circuit. This is suitable for low energy application .Also the realization of CMOS full adder given even better calculation of power delay product by rising using 70nm CMOS technology. The minimum power consumption 1 bit full adder circuit is suitable for 1.2v voltage supply .The proposed circuit improve speed of a full adder circuit.

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