ANALYSIS AND SIMULATION OF DYNAMIC COMPARATOR USING 180NM AND 90NM TECHNOLOGY

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ABSTRACT

In today's world there is demand of low power and high speed application circuits for the portable devices. To meet this demand dynamic comparator play very important role. It has application mostly in Flash ADC. In my paper, I have Analyzed basic dynamic comparator with different characteristics like Propagation delay, speed, offset, ICMR, slew rate etc. I have used TSMC 180nm and TSMC 90nm technology for simulation and compared woks of both technologies. Finally with optimization of these circuits and comparison of these technologies will helped me in obtaining one circuit which will have low power, low offset and high speed CMOS voltage comparator.

KEYWORDS

Dynamic,Transistor, clock, Technology, mismatch, comparator.

1. INTRODUCTION

Dynamic Comparator is one of the basic building blocks in most ADC for application like image sensors, Transceivers etc. Fig 1.Shows the block diagram of Dynamic comparator.

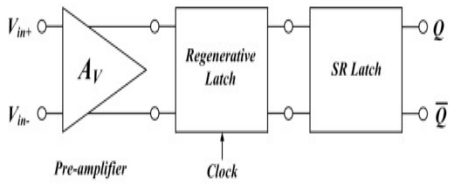

Fig 1. Block diagram of Dynamic Comparator.[02]

In this paper, a Comparator has been analyzed which low power and high speed have compared to existing comparator. There are many types of comparators but Dynamic comparators with their low power are mostly used. It has set of back to back cross coupled inverters to convert a small input-voltage difference to a full scale digital level in a short duration. This paper is divided into six sections. In section-II Conventional Dynamic comparators have been described. Section-III Lewis Comparator, Section- IV Resistor Divider Comparators, Section-V Simulation result, Section-VI Conclusion and Reference.

2. CONVECTIONAL DYNAMIC COMPARATOR

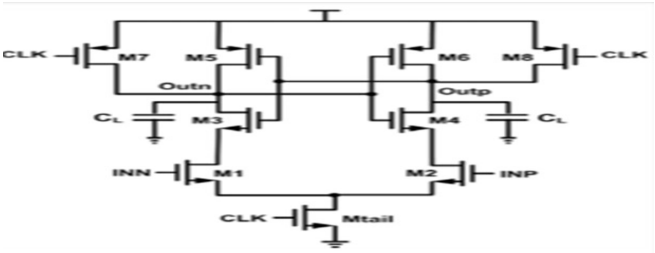

Fig 2.Conventional Dynamic Comparator [03]

The conventional dynamic comparator shown in above fig.2 is mostly used in analog and digital converters. When CLK=0. Called reset phase the transistor M_{tail} will be off. The transistors M5 and M6 which are called reset transistors becomes on and makes the output nodes "outp" and 'outn' to turn into level VDD for beginning of a start condition. When CLK becomes VDD then the M5 and M6 transistors are off, and Mtail becomes on then the output voltages (outp and outn), which where at VDD start to fall with different rates based on the corresponding discharging rates. Assume the case where the voltage VINP is greater than VINN then the voltage at output node discharges faster than the voltage at Outn node. As the voltage at Outp node which is discharged by M2 transistor drain current then voltage goes down to VDD-Vthp before the voltage at Outn node which is discharged by M1 transistor drain current, accordingly M7 transistor becomes on. Thus, the back to back inverters start the latch generation and the voltage at outn node becomes VDD and the voltage level at out node falls down to ground. [03]

3. LEWIS GRAY COMPARATOR

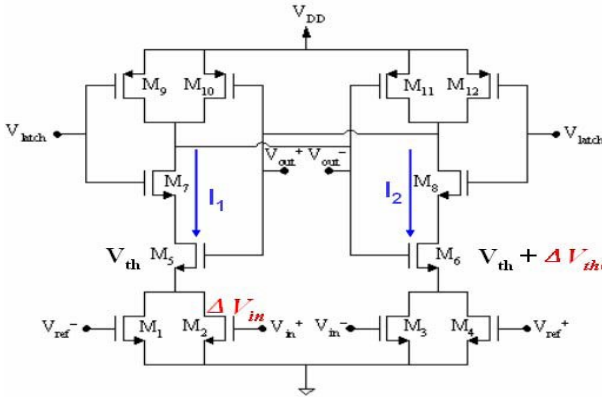

Fig 3. Lewis Gray Comparator [05]

In this structure (Fig.3) of lewis gray comparator input is given through-NMOS M1-M4 which will work in Triode region. The Vin voltage will vary transconductance of M5 & M6. PMOS M10, M11 are latch transistors. M9 & M12 are used as reset latch by setting the Vds of M7 & M8 to zero. Here drain current of M5 & M6 determine final state when latch goes high. If no mismatch is present in the comparator then changes its output when the conductance of the left and right input branches are equal $g_L = g_R$. With the help of threshold voltages of M5 and M6.

$$Vin(Threshold) = \frac{WB}{WA} Vref \qquad \text{----------(01)}$$

Where

$W_A=W_2=W_3$ $W_B=W_1=W_4$

$V_{IN=}V_{in1} - V_{in2}$ $V_{ref}=V_{ref1} -V_{ref2}$

In Evaluation phase $V_{latch}= V_{DD}$ & M_{10} and M_{11} both PMOS transistors have equal drain and gate voltage, which make them both work at saturation region. Transistors M_7 and M_8 work as switches in cross-coupled transistor pairs including M_5M_{10} and M_6M_{11}.This all are turned on during comparison stage and also working in the triode region because of its high gate voltage $V_{g7,8} = V_{DD}$. The drain voltage of M_5 and M_6 is pulled up closed to V_{out+} or V_{out-} and works in saturation because switches M_7 and M_8 are in the triode region. Transistors M_9 and M_{10} are both turned off because control signal V_{latch} is V_{DD}, which indicates that mismatch effects in M_9 and M_{12} is negligible [05].

4. RESISTER DIVIDER COMPARATOR

As shown in Fig, 4 is called Resister divider comparator because the input pairs (M1-M4) operate in linear region and adjust the trip point of the comparator resistively by means of

$$Vin1 - Vin2 = \frac{B1}{B2}(Vref1 - Vref2) \qquad \text{…….(02)}$$

Where

B1= μnCoxW1/L1= μnCoxW2/L2

B2= μnCoxW3/L3= μnCoxW4/L4

This comparator is widely used because of its low kickback noise and simple relationship between input voltage and reference voltage as expressed in equation-(02). Additionally input can be as low as threshold voltage, Vthn and there for it can be used in low supply voltage. However, since M1- M4 are in deep linear region. The input referred offset is sensitive to the device mismatch of M1- M4 and M5- M6.This type of circuit will have more offset. [04]

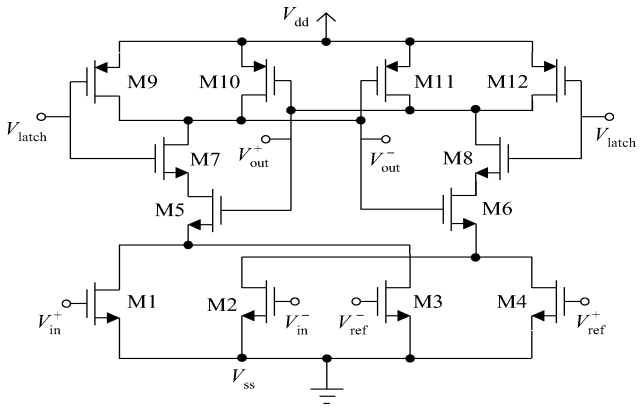

Fig 4.Resister Divider [04]

5. SIMULATION AND RESULT

(1) The simulation of the above three dynamic comparators is done using 180nm TSMC and 90nm Generic technologies. The supply voltages used are 0.5V for 90nm and 1.8V for 180nm technology as shown in Table II.
(2) Transistor dimensions are presented in Table III. Table. I.A&B shows the comparator performance in terms of Propagation delay, offset voltage, ICMR and speed, slew rate etc. for 90nm & 180nm.
(3) For Simulation I have used Tanner Tools Version 13.00, with the help of S-Edit v13.00 T-Spice v13.00 and W-Edit v13.00 applications.
(4) Simulated Output waveforms of Conventional dynamic comparator, Resistor Divider and Lewis gray comparators are illustrate in Fig .5, Fig.7 and Fig.9.with their input pulses using Generic 90nm Technology.Fig.No.6,8&10shows the offset voltages of Conventional dynamic comparator, Resistor Divider and Lewis gray comparators simulated using Generic 90nm technology. There values are mentioned in Table I.B.

Parameter	**Lewis Gray Comparator**	**Simple Dynamic Comparator**	**Resistive Comparator**
	180 nm	**180 nm**	**180 nm**
Propagation Delay (ns)	2.01ns	2.55ns	2.03ns
ICMR	1.54V to 1.64 V	-1.75 V to 1.60 V	1.79990V to 1.79980 V
Offset Voltage (mV)	260.08mv	942.46mv	1.14 V
Slew rate	79.35mv/ns	3.37mv/ns	10μv/ns
Speed	50MHz	390MHz	50MHz

Table I.A Comparative Analysis of above circuits.

Parameter	**Lewis Gray Comparator**	**Simple Dynamic Comparator**	**Resistive Comparator**
	90 nm	**90 nm**	**90 nm**
Propagation Delay (ns)	1.55ns	1.8ns	1.8ns
ICMR	492.42 mV to 492.36 mV	-0.5Vto 0.5V	484.90mV to 497.49mV
Offset Voltage(mV)	150.62 mV	152.41 mV	331.72 mV
Slew rate	943.98mV/ns	955.59 mV/ns	991.76 mV/ns
Speed	640 MHz	150 MHz	550 MHz

Table I.B Comparative Analysis of above circuits.

Voltage Terminals	**Technology**	
	180nm	***90nm***
V_{DD}	1.8V	5v
Vss	-1.8V	-5v
V_{IN+}	1.8 V	0.5
V_{IN-}	-1.8 V	-0.5
V_{latch}	0.9 V	0.1V
$Vref_{\pm}$	±0.5 V	± 0.1v

Table II.Voltage level used during simulation for above circuits.

Types of Circuits/ Transistor	**Lewis Gray**	**Simple Dynamic**	**Resister Divider**
	180nm	180nm	180nm
M1	N-10u	N-03u	N-10u
M2	N-10u	N-03u	N-10u
M3	N-10u	N-03u	N-10u
M4	N-10u	N-03u	N-4u
M5	N-06u	P-03u	N-5.5u
M6	N-06u	P-03u	N-5.5u
M7	N-03u	P-05u	N-5.5u
M8	N-03u	P-05u	N-5.5u
M9	P-5.5u	N-2.5u	P-15u
M10	P-2.5u	X	P-10u
M11	P-2.5u	X	P-10u
M12	P-5.5u	X	P-15u

Table III-A Transistor Dimension

Types of circuits/ Transistor	**Lewis Gray**	**Simple Dynamic**	**Resister Divider**
	90nm	**90nm**	**90nm**
M1	N-3.5u	N-2u	N-2u
M2	N-3.5u	N-2u	N-2u
M3	N-1.5u	N-2u	N-2u
M4	N-1.5u	N-2u	N-2u
M5	N-2u	P-2u	N-3u
M6	N-2u	P-2u	N-3u
M7	N-2u	P-3u	N-3u
M8	N-2u	P-3u	N-3u
M9	P-3.5u	N-3u	P-5.5u
M10	P-15u	X	P-2.5u
M11	P-15u	X	P-2.5u
M12	P-3.5u	X	P-5.5u

Table III-B.Transistor Dimensions

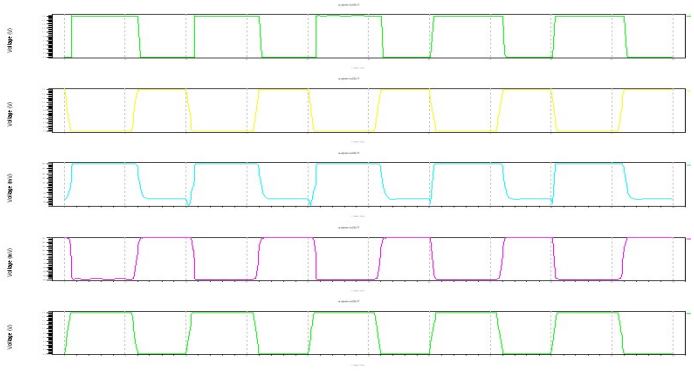

Fig.5 output waveform of Convectional dynamic comparator simulated using 90nm.

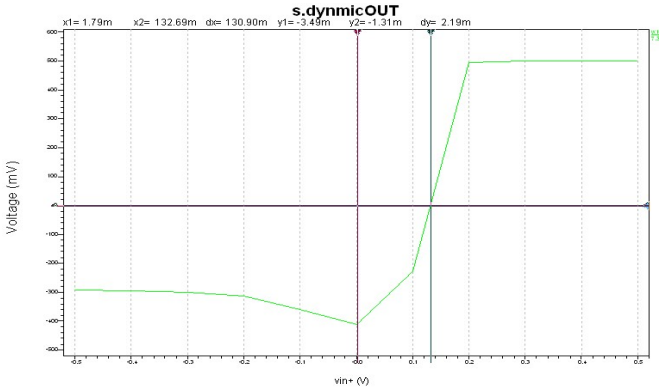

Fig.6. offset voltage of Convectional dynamic comparator simulated using 90nm.

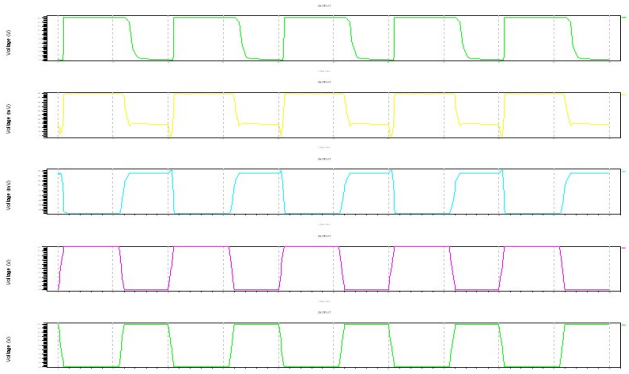

Fig.7.Resistive Divider comparator output waveform simulated using 90nm.

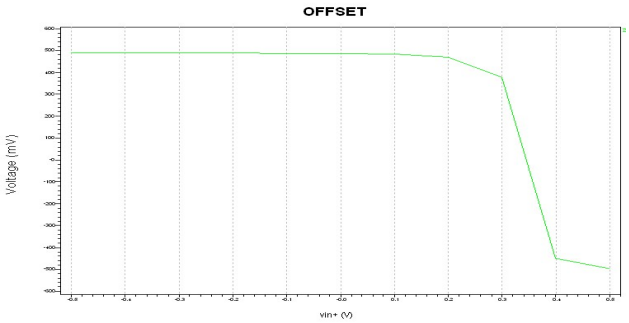

Fig .8. Resistive Divider comparator Offset voltage simulated using 90nm.

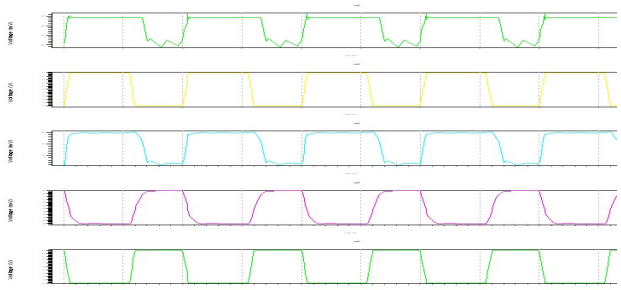

Fig.9.Lewis gray comparator output waveform simulated using 90nm.

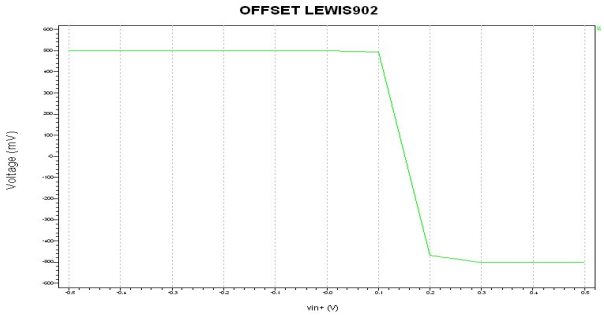

Fig.10. Lewis gray comparator offset voltage simulated using 90nm.

6. CONCLUSION

I conclude that Dynamic comparator can used to obtain low power and high speed CMOS comparator. Also found that with reduction of technology and optimizing the circuit can be obtained which low power, low offset and high speed CMOS voltage comparator. After comparing result of 180nm with 90nm dynamic comparators results are better for 90nm technology. Out of three comparators result of conventional dynamic comparator is better as shown in Table I.

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