PERFORMANCE ANALYSIS OF LOW POWER FULL ADDER CELLS USING 45NM CMOS TECHNOLOGY

K.Dhanunjaya[1], Dr.MN.Giri Prasad[2], Dr.K.Padmaraju[3]

1. Research scholar, JNTUA Anatpuramu, A.P, INDIA.
2. Professor, Department of ECE, JNTUA, Anatapuramu, A.P, INDIA.
3. Professor, Deparment of ECE, JNTUK, Kakinada, A.P, INDIA.

ABSTRACT

This paper puts forward different low power adder cells using different XOR gate architectures. Adder plays an important role in arithmetic operation such as addition, subtraction, multiplication, division etc. The optimization and characterization of such low power adder designs will aid in comparison and choice of adder modules in system design. A comparative analysis is performed for the power, delay, and power delay product (PDP) optimization characteristic& deals with the design of five adder cells using transistors and schematic structure using CADENCE tool. 10 transistor adder circuits shows the least power consumption with others. Simulations are performed by using Cadence Design tools using 45nm CMOS technology. The four adder cell module proposed here demonstrates their advantages in comparison with Static Energy Recovery Full (SERF), including lower power consumption, smaller area, and higher speed at different frequencies.

Keywords

Low power, Static Energy Recovery Full Adder (SERF), 45 nm technology, power delay product (PDP).

1. INTRODUCTION

The 1-bit full adder cell is the building block in majority of the VLSI applications, such as digital signal processing, image and video processing, microprocessors & common use calculation operations. Also, multiplication and subtraction are examples of the most commonly used operations in various logic design modules. Therefore, its performance improvement is acute for enhancing the overall module efficiency.

Moreover low-power VLSI systems have emerged into great demand because of the fast growing technologies in mobile communication and computation. The battery technology doesn't advance at the same rate as high as the microelectronics technology. For the mobile systems a limited amount of power is sourced. So challenging constraints of designers facing are: high speed, high throughput, small silicon area, and at the same time, low-power consumption. So, building high- performance, low-power adder cells is of great interest.

2. Basic Adder cell equation

1-bit full adder (1) which has three 1-bit inputs (A, B and C) and two 1-bit outputs (Sum and carry). The relations between the inputs and the outputs are expressed as:

$$Sum = A \oplus B \oplus C_{in} \quad .. (1)$$
$$C_{out} = A.\ B + C_{in}.\ (A+B) \ .. \ (2)$$

There are many logic styles for designing digital circuits which mainly influences the circuit performance. A gate is evaluated by three basic parameters, area, delay time (propagation delay) and power consumption. Depending on the application, the emphasis will be on different parameters. The delay time depends on the size and number of transistors, the parasitic capacitance including intrinsic capacitance and capacitance due to routing and the number of logic gates. The power consumption depends on the switching activity, size and number of transistors, glitch, leakage current of transistors and sub-threshold current.

Power consumption in CMOS digital circuits is divided into three main parts as follows:

$$P_{Total} = P_{Dynamic} + P_{Static} + P_{Short\text{-}circuit} \ldots. \quad (3)$$

- Due to charging and discharging capacitances.
- Due to the current between power supply and ground during a transistor switching.
- Due to the leakage current and static current.

3. Different Full Adder circuits

Different types of full adder circuits analyzed in this paper are

3.1. Conventional 28T CMOS Full Adder Circuit

The conventional CMOS adder cell using 28 transistors based on standard CMOS topology is shown in fig.1. Due to high number of transistors, its power consumption is high. Large PMOS transistor in pull up network results in high input capacitances, which causes high delay and dynamic power. This is reliable because it possesses a high noise margin, which is considered to be the most significant advantage of the full adder.

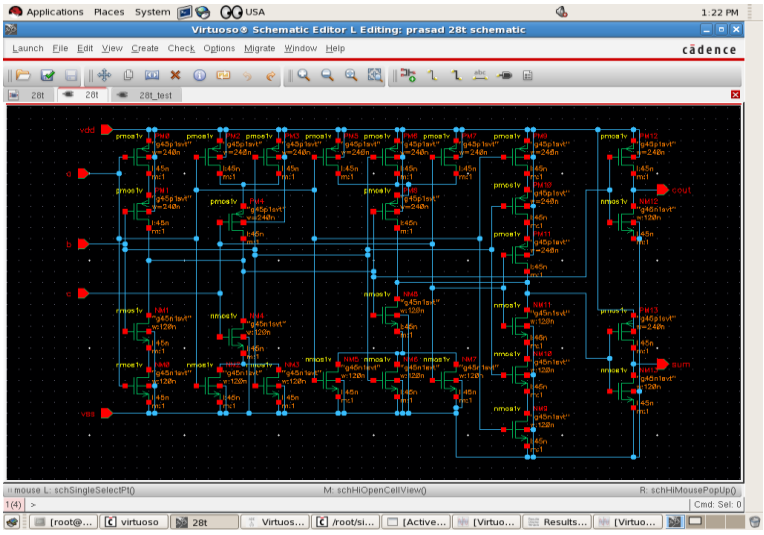

Figure 1: CMOS 28 transistor Full adder

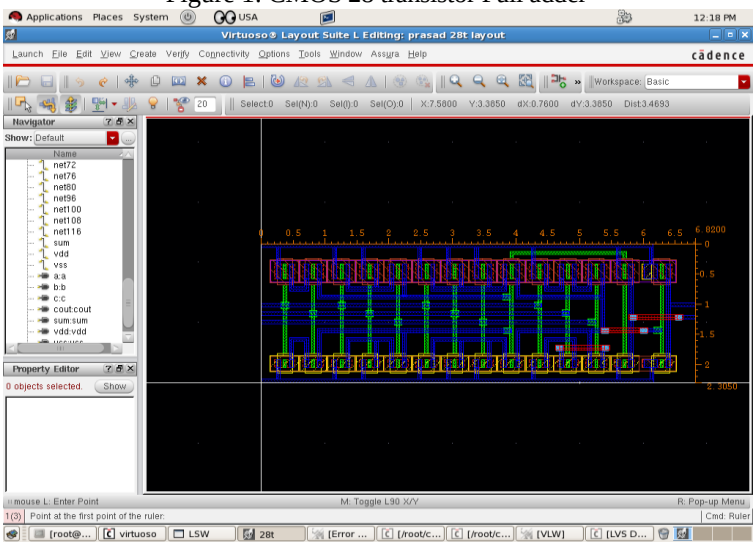

Figure 2: Layout of CMOS 28 transistor Full adder

3.2. 8T Adder circuit

Figure.3 shows schematic and Figure.4 shows layout of 8T full adder cell (6) designed using CMOS 45 nm technology consist eight transistors which possess different width properties. The sum is generated using six transistors from which three transistors act as one XOR gate, thus the result is applied to another XOR gate made up of three transistors. The carry is resulted from the remaining two transistors the result of first XOR gate acts as control input of two combined transistors. It consumes high power as it has different width properties.

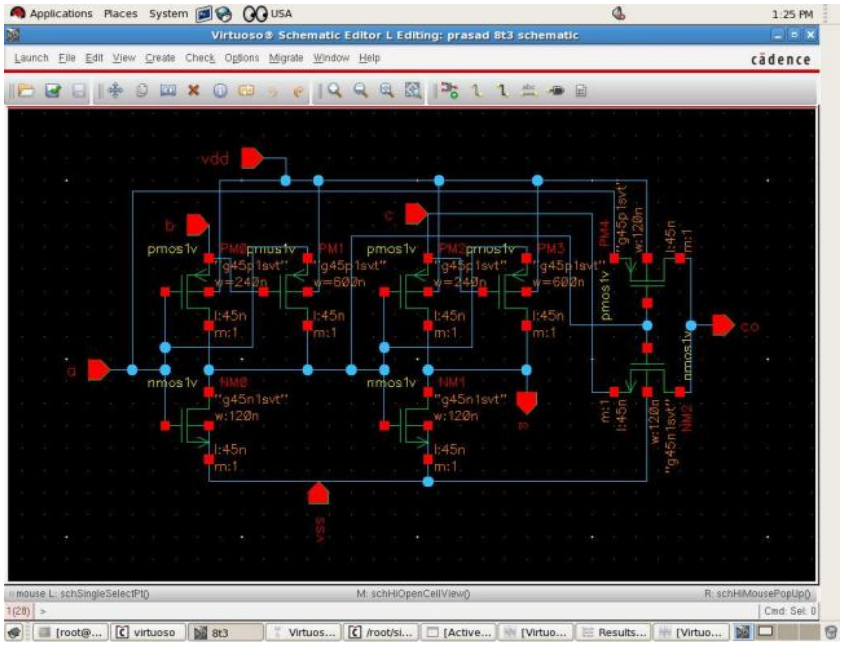

Figure 3: Schematic of CMOS 8T Full adder

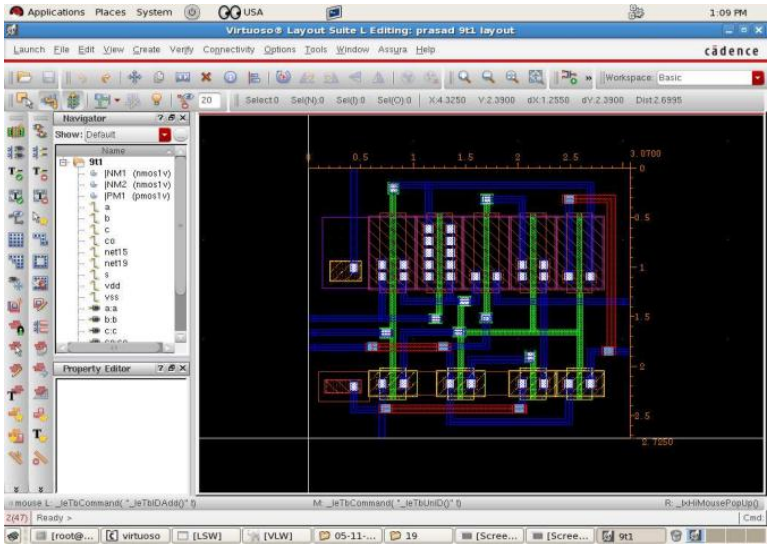

Figure 4: Layout of CMOS 8T Full adder

3.2.9 T Full Adder

Figure.5 shows schematic and Figure.6 shows layout of 9T full adder cell designed using CMOS 45 nm technology consist nine transistors and the transistors have different width properties. The sum is generated using six transistors from which three transistors acts as one XOR gate, the result is applied to another XOR gate made up of three transistors. The carry is a result of the remaining two transistors- the result of first XOR gate acts as control input of two combined

transistors. It consumes high power as it is of different width properties. The transistor left is used at the bottom of the second XOR gate that reduces the leakage power. The power consumption reduces comparatively as of 8T adder.

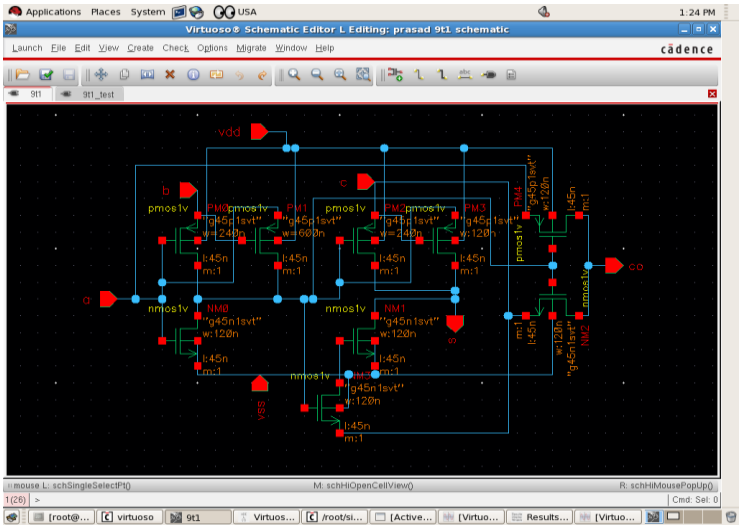

Figure 5: Schematic of CMOS 9T Full adder

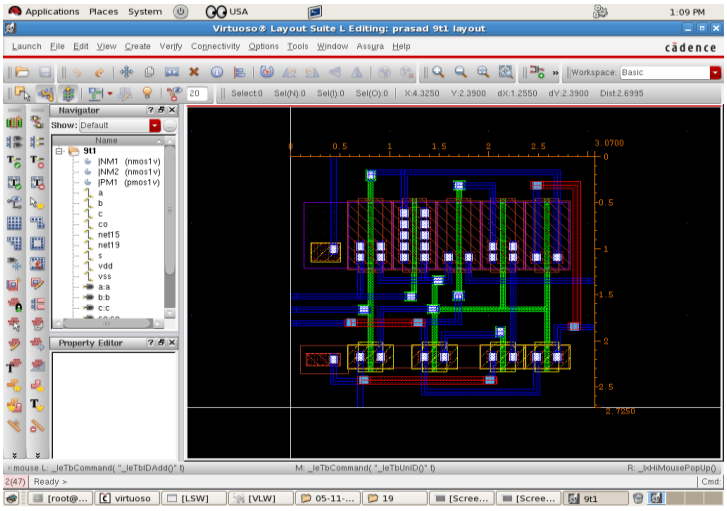

Fig. 6 Layout of CMOS 9T Full adder

3.4. SERF Full Adder

Figure.7 shows schematic and Figure.8 shows layout of SERF full adder cell (5) designed using CMOS 45 nm technology is energy recovering logic consumes less power than non- energy recovering logic as it reuses charge. In this type of adder the energy recovering logic reuses charge and therefore consumes less power than non-energy recovering logic. It has two XNORs

realized by 4 transistors. Sum is generated from the output of the second stage XNOR circuit. The Cout can be calculated by multiplexing ‘a’ and ‘cin’ controlled by (a ⊗ b).

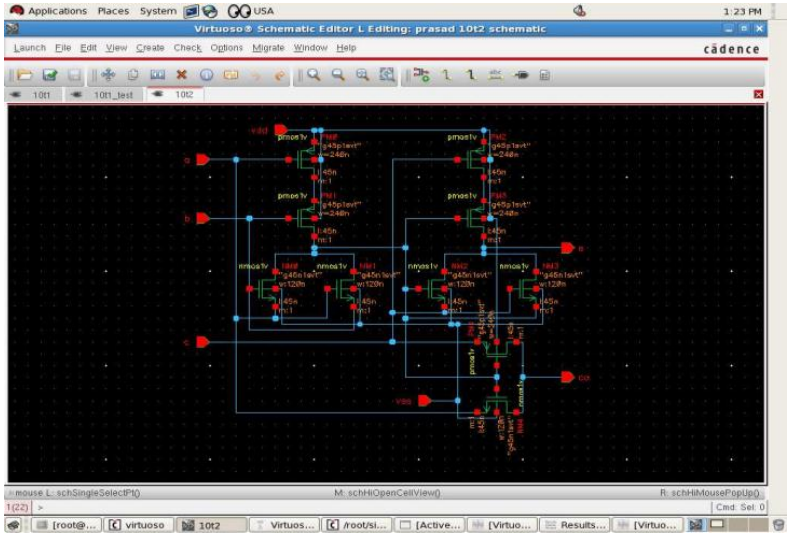

Figure 7: Schematic of SERF adder

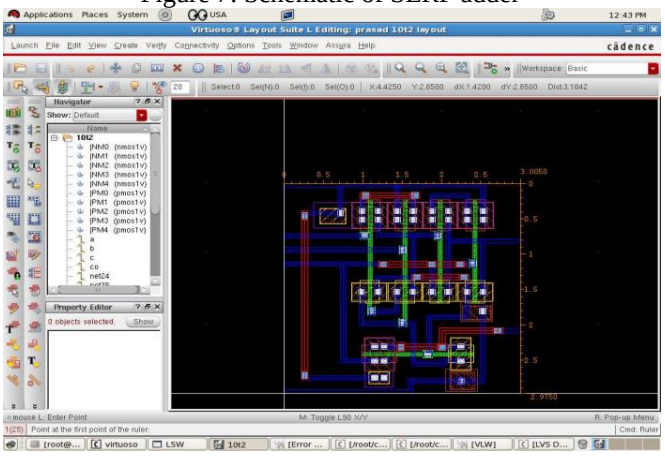

Figure 8: Layout of SERF adder

3.5 10T adder

Figure.9 shows schematic and Figure.10 shows layout of 10T full adder (2) cell designed using CMOS 45 nm technology consist energy recovering logic reuses charge and therefore consumes less power than non-energy recovering logic. The circuit consists of two XORs realized by 4 transistors. Sum is generated from the output of the second stage XOR circuit. The C_{out} can be calculated by multiplexing ‘a’ and ‘C_{in}’ controlled by (a ⊗ b). Let us consider that there is a capacitor at the output node of the first XOR module.

It is identified that the new 10T adder receives less power from VDD than SERF. The charge stored at the load capacitance is reapplied to the control gates. The combination of not having a direct path to ground (depends on input) and the re-application of the load charge to the control gate makes the 10T full adder an energy efficient design. The circuit produces full-swing at the output nodes. But somewhat less to provide so for the internal nodes. As the power consumption by the circuit is less so it is used in low power applications.

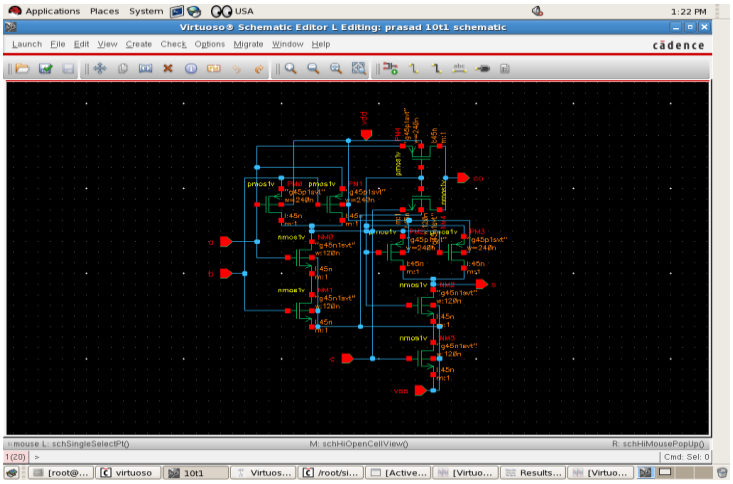

Figure 9: Schematic circuit of 10T adder

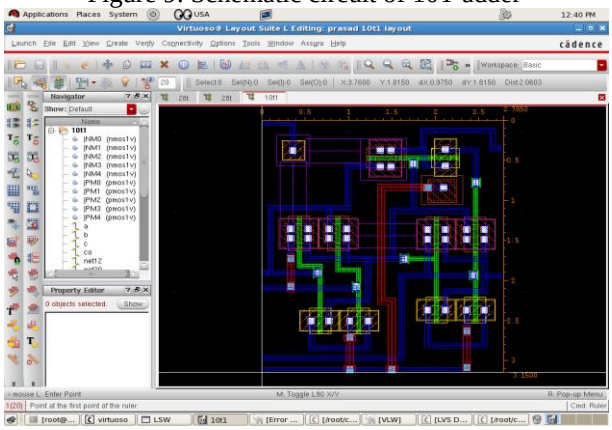

Figure 10: Layout of 10T adder

4. Characteristics of the proposed full adders

4.1. Dynamic Power

The total power dissipated in CMOS circuits is composed of two parts. One is static power consumption the other is dynamic power dissipation. In 45 nm transistor technology, the static power loss is far less than its counterpart dynamic power dissipation. In majority

applications, the total power loss is approximate to dynamic power consumption, which is related to the probability of switching and the internal node capacitance.

4.2. Short Circuit Current

Short circuit current occurs when both NMOS and PMOS transistors are consecutively active. The direct current flows through the supply and the ground. This is quite low in all the proposed adder circuits.

5. Simulation and Comparison

5.1. Simulation Environment

The proposed five low power full adders cells are simulated and Layout is constructed using virtuoso in Cadence design Tools. The parameters are extracted with 45nm (GPDK45) CMOS technology at different supply voltages and frequencies.

5.2. Comparison of Different adder cells

The performance of CMOS circuits is rated with Power consumption and working speed. The proposed five full adder's performances at different frequencies and supply voltages are shown from sec 5.2.1 to 5.2.5 indicates power measured from layout of adder cell and power delay product (PDP).

Power-Delay product is another important factor for CMOS circuits. This is applied often in testing characteristics of CMOS circuits. In majority circuits, requirements of low power and high speed cannot be accomplished simultaneously, comparisons only using these two metrics may become complex.

5.2.1 Performance of 28T Adder cell:

Table: 1 & Figure 11 Shows power comparison of 28T adder cell at different supply voltages and frequencies. Table: 2 & Figure 12 Shows Power Delay Product comparison of 28T adder cell at different supply voltages and Frequencies.

Layout average power(nW)					
Supply voltage(V)	Frequency(MHz)				
	100	200	250	400	500
0.8	369.8	735.4	917.2	1460	1820
1.0	591.6	1180	1472	2347	2928
1.2	866.9	1731	2161	3449	4305

Table 1. Power consumption of 28T adder

Layout Power Delay Product(aW-S)					
Supply voltage(V)	Frequency(MHz)				
	100	200	250	400	500
0.8	204.806	407.287	507.973	808.592	1007.971
1.0	146.965	293.136	365.674	583.042	727.374
1.2	141.582	282.707	352.935	563.291	703.093

Table 2. PDP of 28T adder

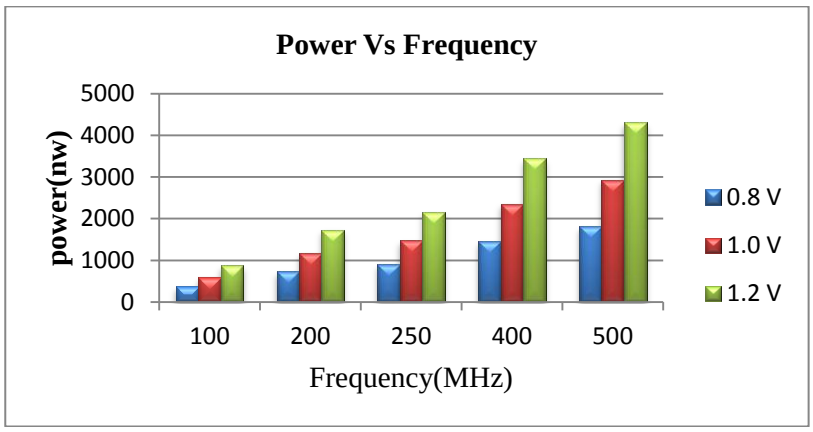

Figure 11: Power comparison of 28T adder at 0.8 V, 1.0 V & 1.2 V supply voltage

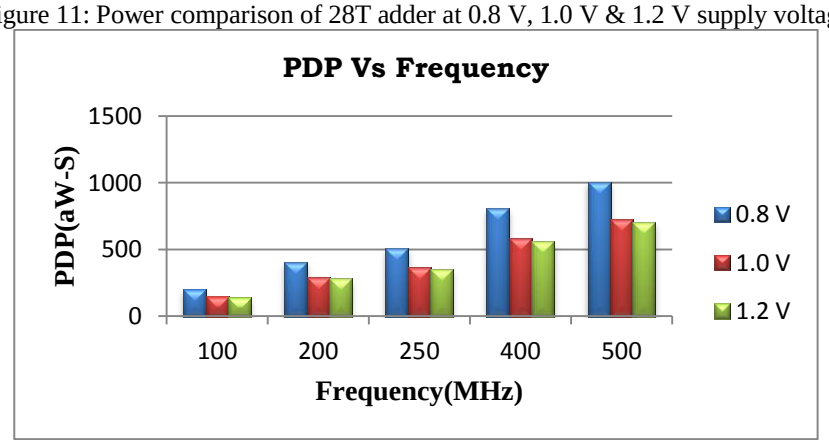

Figure.12: PDP of 28T adder at 0.8 V, 1.0 V & 1.2 V supply voltage.

5.2.2 Performance of 8T Adder cell:

Table: 3 & Figure 13 Shows power comparison of 8T adder cell at different supply voltages and frequencies. Table: 4 & Figure 14 Shows Power Delay Product comparison of 8T adder cell at different supply voltages and Frequencies.

Layout Average Power(µW)					
Supply Voltage(V)	Frequency(MHz)				
	100	200	250	400	500
0.8	5.671	5.744	5.78	5.89	5.963
1.0	17.69	17.79	17.84	17.99	18.09
1.2	35.87	36.0	36.06	36.26	36.39

Table 3: Layout power consumption of 8T adder

Layout Power Delay Product(fW-S)					
Supply Voltage(V)	Frequency(MHz)				
	100	200	250	400	500
0.8	12.176	12.332	12.410	12.646	12.803
1.0	10.131	10.188	10.217	10.303	10.360
1.2	6.783	6.808	6.819	6.857	6.881

Table 4. PDP of 8T adder

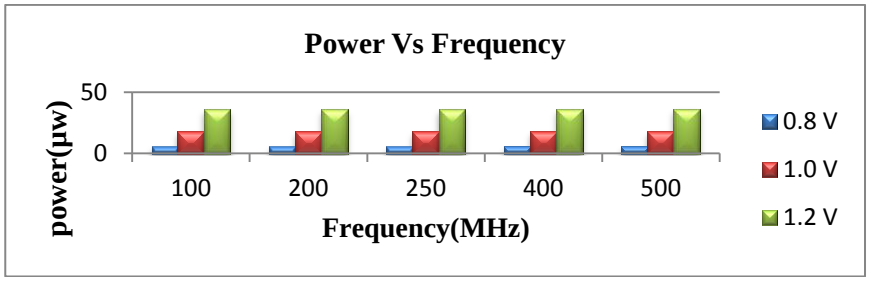

Figure 13: Power comparison of 8T adder at 0.8V,1V &1.2 V supply voltage

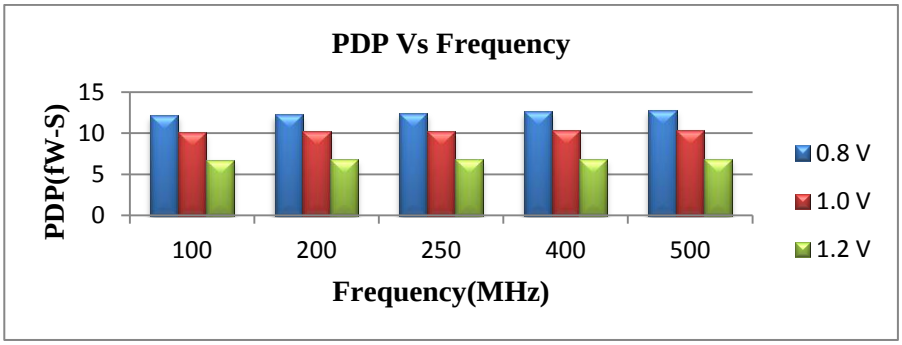

Figure 14: PDP comparison of 8T adder at 0.8V,1V &1.2 V supply voltage

5.2.3 Performance of 9T Adder cell:

Table: 5 & Figure 15 Shows power comparison of 9T adder cell at different supply voltages and frequencies. Table: 6 & Figure 16 Shows Power Delay Product comparison of 9T adder cell at different supply voltages and Frequencies.

Layout Average Power(µW)					
Supply Voltage(V)	Frequency(MHz)				
	100	200	250	400	500
0.8	3.81	3.868	3.896	3.981	4.038
1.0	11.52	11.63	11.68	11.84	11.94
1.2	22.75	22.86	22.93	23.18	23.34

Table 5: Layout power consumption of 9T adder

Layout Power Delay Product(fW-S)					
Supply Voltage(V)	Frequency(MHz)				
	100	200	250	400	500
0.8	9.495	9.639	9.709	9.921	10.063
1.0	32.970	33.285	33.428	33.886	34.172
1.2	22.345	22.453	22.522	22.767	22.925

Table 6. PDP of 9T adder

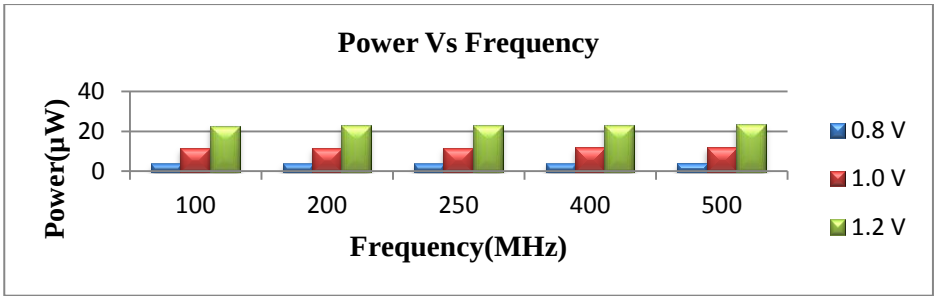

Figure 16: Power comparison of 9T adder at 0.8V,1V &1.2V supply voltages

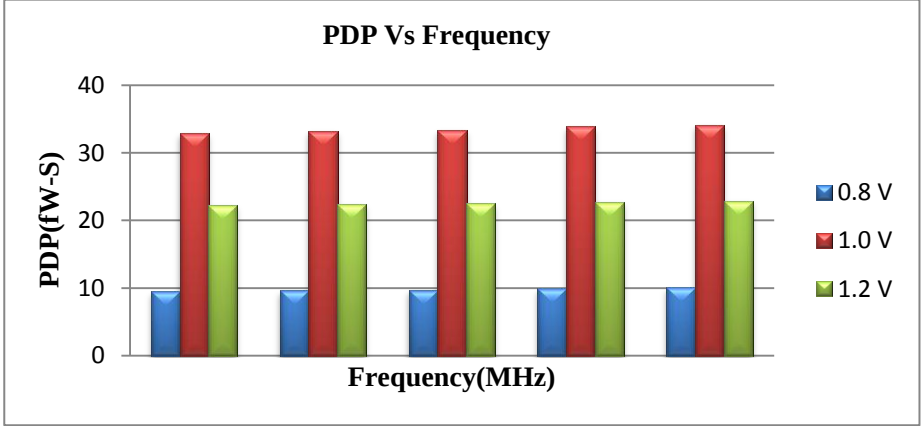

Figure 17: PDP comparison of 9T adder at 0.8V, 1V &1.2V supply voltages

5.2.4 Performance of SERF Adder cell:

Table: 7 & Figure 17 Shows comparison power consumption of SERF adder cell at different supply voltages and frequencies. Table: 8 & Figure 18 Shows Power Delay Product comparison of SERF adder cell at different supply voltages and Frequencies.

Layout Average Power(nW)					
Supply Voltage(V)	Frequency(MHz)				
	100	200	250	400	500
0.8	115.8	221.2	274.2	433.0	538.3
1.0	207.3	401.5	495.8	768.9	935.2
1.2	325.0	627.0	775.0	1211	1497

Table 7: Layout Power consumption of SERF adder

Layout Power Delay Product(fW-S)					
Supply Voltage(V)	Frequency(MHz)				
	100	200	250	400	500
0.8	90.046	172.005	213.218	336.701	418.582
1.0	99.836	193.362	238.777	370.302	450.392
1.2	48.110	92.815	114.723	179.264	221.601

Table 8. Layout PDP of SERF adder

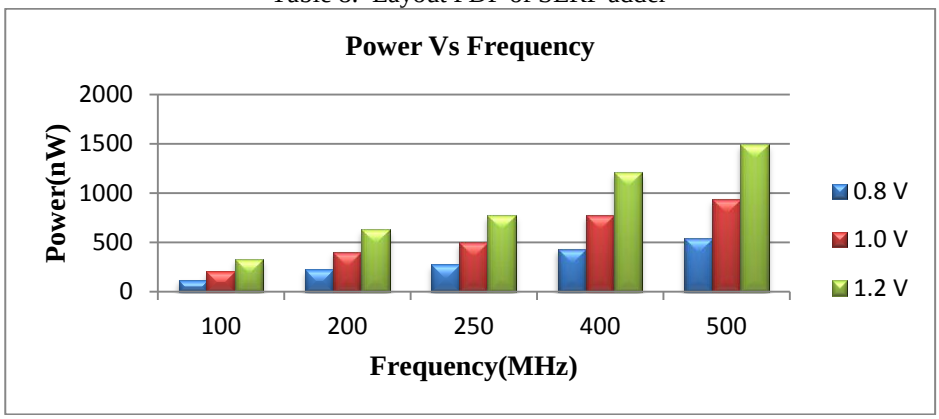

Figure 17: Power comparison of SERF adder at 0.8V,1V & 1.2V supply voltages

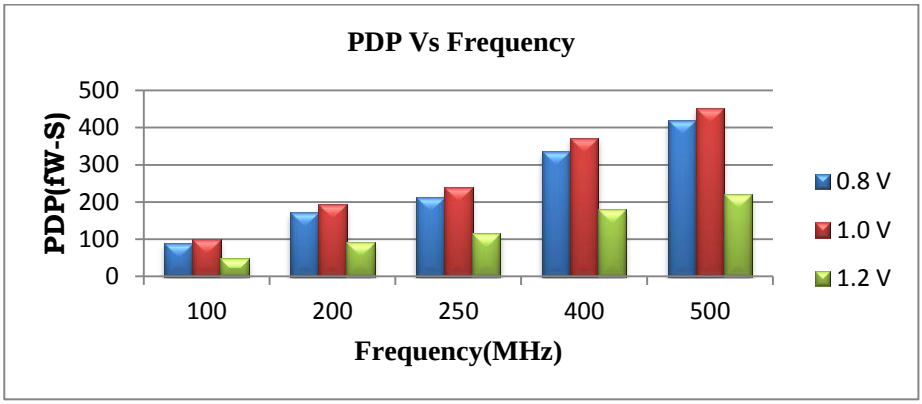

Figure 18: PDP comparison of SERF adder at 0.8V,1V & 1.2V supply voltages

5.2.5 Performance of 10T Adder cell:

Table: 9 & Figure 19 Shows comparison power consumption of 10T adder cell at different supply voltages and frequencies. Table: 10 & Figure 20 Shows Power Delay Product comparison of 10T adder cell at different supply voltages and Frequencies.

Layout Average Power(nW)					
Supply Voltage(V)	Frequency(MHz)				
	100	200	250	400	500
0.8	108.5	217.0	271.1	433.3	541.2
1.0	167.1	334.0	417.3	667.4	834.1
1.2	237.0	472.9	589.8	942.5	1180

Table 9: Layout Power consumption of 10T adder

Layout Power Delay Product(fW-S)					
Supply Voltage(V)	Frequency(MHz)				
	100	200	250	400	500
0.8	69.060	138.121	172.555	275.795	344.474
1.0	18.849	37.675	47.071	75.283	94.086
1.2	8.532	17.024	21.233	33.930	42.480

Table 10: Layout PDP of 10T adder

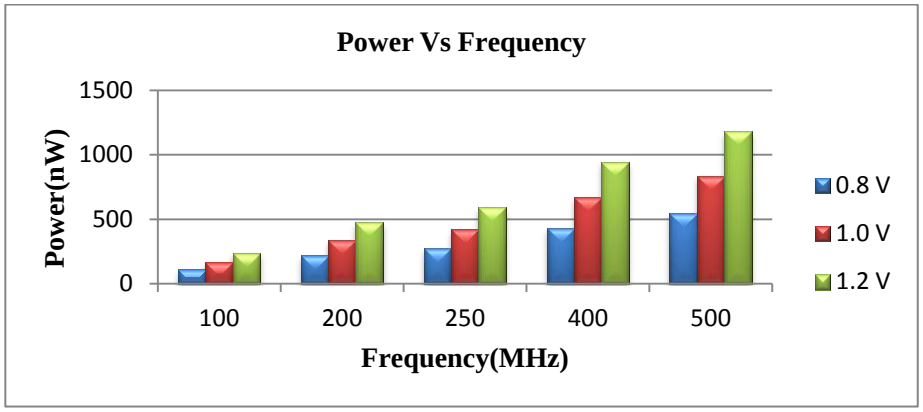

Figure 19: Power comparison of 10T adder at 0.8V, 1V & 1.2V supply voltages

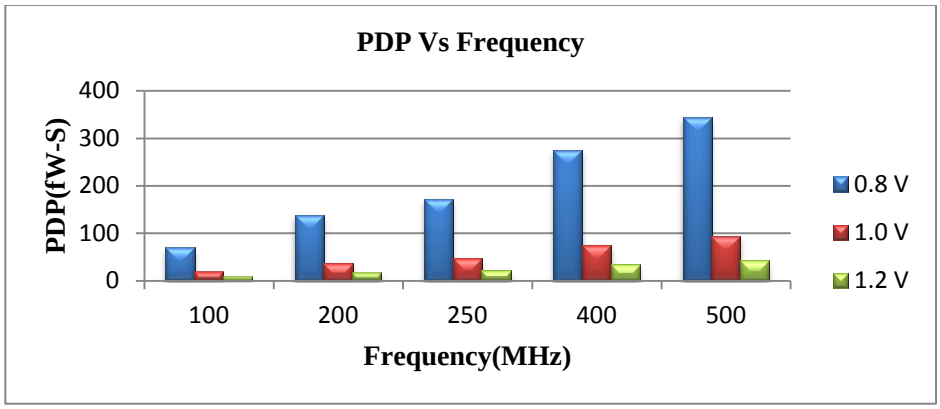

Figure 20: PDP comparison of 10T adder at 0.8V, 1V & 1.2V supply voltages

6. CONCLUSION

From the power & delay analysis of five full adder cells designed in 45 nm CMOS technology at different supply voltages and frequencies concluded that they possess the merits of low power depletion, small delay, small Power-Delay product, and area saving due to lower transistor counts and special structures. The simulation results demonstrate that these five proposed full adder cells can be better alternatives in divergent fields for various uses at different frequencies and at different supply voltages. It is concluded that 10T Adder cell is fit for delay and power centric design.

7. REFERENCES:

[1] Sreehari Veeramachaneni and Hyderabad, "New improved 1-bit adder cells", CCECE/CCGEI, Niagara Falls. Canada, May 5-7 2008, pp. 735-738.

[2] Po-Ming Lee, Chia-Hao Hsu, and Yun-Hsiun Hung, "Novel 10-T full adders realized by GDI structure", 2007 IEEE International Symposium on Integrated Circuits (ISIC-2007), pp. 115-118.

[3] Alireza Saberkari, Shahriar Baradaran Shokouhi, "A novel low-power low-voltage CMOS 1-bit full adder cell with the GDI technique",2006 IJME- INTERTECH Conference.

[4] A. Morgenstern, A. Fish, I. A. Wagner, "Gate Diffusion Input (GDI) – A Novel Power Efficient Method for Digital Circuits: A Design Methodology," 14th ASIC/SOC Conference, Washington D.C., USA, September 2001.

[5] R. Shalem, E. John, and L. K. John, "A novel low power energy recovery full adder cell", in Proc. IEEE Great Lakes VLSI Symp., pp.380-383, Feb. 1999

[6]. Yi WEI, Ji-zhong SHEN, "Design of a novel low power 8-transistor 1-bit full adder cell", Journal of Zhejang University-SCIENCE C (Computers and Electronics), 2011 12 (7): 604-607, ISSN 1869-1951(Print).

[7]. Deepa Sinha, Tripati Sharma, K. G. Sharma, Prof. B. P. Singh, "Ultra Low Power 1-Bit Full Adder", International Symposium on Devices MEMS, Intelligent Systems & communication (ISDMISC) 2011, Proceedings Published by International Journal of Computer Applications (IJCA).

[8]. L. Junming et al., "A novel 10-transistor low-power high-speed full adder cell", Proceedings of 6th International Conference on Solid-State and Integrated-Circuit Technology (2001), pp.1155–1158

[9]. Dhireesha Kudithipudi and Eugene John, "Implementation of Low Power Digital Multipliers Using 10 Transistor Adder Blocks", Journal of Low Power Electronics, Vol.1, 1–11, 2005.

[10]. D. Radhakrishnan, "Low Voltage CMOS Full Adder Cells", Electronics letters (1999), Vol.35, p.1792–1794.

[11]. L. Junming, S.Y an, L. Zhenghui, and W. Ling, "A novel 10-transistor low- power high-speed full adder cell", Proceedings of 6th International Conference on Solid-State and Integrated-Circuit Technology (2001), pp.1155–1158.