A NOVEL CMOS DYNAMIC LATCH COMPARATOR FOR LOW POWER AND HIGH SPEED

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ABSTRACT

This paper presents a novel dynamic latched comparator that consumes lower power and higher speed than the conventional dynamic latched comparators. This paper also provides a comprehensive review of a variety of comparator designs in terms of power and delay. The comparators and the proposed circuit are designed and simulated their transient responses in Tanner EDA suite using 180 nm CMOS technology and 1V power supply voltage and it demonstrates up to 0.03968 mill watt power consumption and higher speed with delay of 60.29 picoseconds than the conventional latched comparators.

KEYWORDS

Latch comparator, low-power high speed, dynamic comparator.

1. INTRODUCTION

The power problem is one of the most serious limitations in high performance VLSI's and battery backed-up systems. High speed and low power comparators are the essential building blocks of many analog circuits such as high speed analog-to-digital converters (ADCs), memory sense amplifiers and data receivers. In analog to-digital converters, the comparator plays a vital role on the overall performance of the converter. A fast and accurate comparator is a crucial element in any high resolution and high speed data converters. There are two main types of comparator based on their structure and operation: amplifier chain type and latch type. Amplifier chain-type comparators use a set of cascade amplifiers to generate the output in response to small difference between input signal and reference signal. On the other hand, latch type comparators provide higher speed and lower power consumption.

A common architecture used in analog circuits is dynamic latch. It has excellent speed alongwith an acceptable accuracy. In the past preamplifier based comparators have been used for ADC architecture such as flash and pipeline [5]. The main drawback of preamplifier based comparators is the offset voltage. This drawback is overcome in dynamic latch comparator as it makes a comparison once in every clock cycle and require much less offset voltage. However this dynamic latch comparator suffers from larger power dissipation than preamplifier based comparators.

Another disadvantage of dynamic latch is the kickback noise produced by high transition current. This noise produced induces voltage spikes at the voltage differential input signal. This voltage difference can toggle the comparator output resulting in comparison errors. Some researchers have proposed topologies which can reduce the effect of kickback noise with the addition of a gain stage between the latch and the preamplifier.

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2. METHODOLOGY

2.1 Basic Dynamic Latch

A dynamic latch consists of two cross-coupled inverters. Figure 1 shows the schematic of a basic dynamic latch. When V_{out+} increase (V_{out-} decreases), transistor M2 increases the current drawn from V_{out-} node, and thereby decreasing its voltage. As a result, the transistor M1 will have reduced gate to source voltage, V_{gs}, thus, decreasing the current through M1, causing voltage at V_{out+} to increase. The PMOS transisitors have similar function. The use of combination of PMOS and NMOS transistor reduces the time constant by 25% compared to single regeneration part.

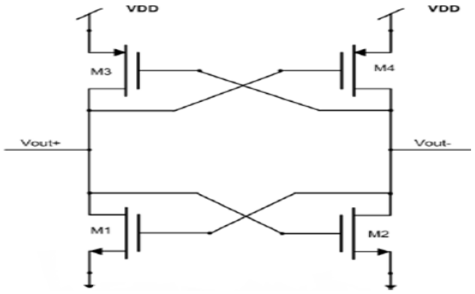

Fig 1. Basic dynamic latch

2.2 Preamplifier-Latch Principle

The basic principle is that the preamplifier amplifies the input signal, and this amplified signal then goes to the latch stage. The offset voltage is divided by the gain, A_v of preamplifier and converted in the input. Hence, the offset voltage is reduced and it lies mostly in the preamplifier stage.

2.3 Offset Voltage in Dynamic Latch

The offset voltage in dynamic latch is given as [1]:

$$V_{OFFSET} = \nabla V_{TH} + \frac{1}{2}\left[\frac{\nabla W}{W} - \frac{\nabla L}{L}\right](V_{GS} - V_{TH}) + \frac{\nabla Q}{C_D}$$

Where ∇V_{TH} is the standard deviation of the threshold voltage, $\nabla W/W$ is the width mismatch and $\nabla L/L$ is the length mismatch, $V_{GS} - V_{TH}$ is the overdrive voltage, ∇Q is the charge due to switches controlling the $Vout+$ and $Vout-$ node, C_D is the total equivalent output capacitance.

3. PREVIOUS WORKS

3.1 Preamplifier Based Comparator

The circuit basically consists of a preamplifier followed by a double regenerative dynamic latch along with an output buffer stage. The preamplifier used here is self-biased differential circuit with active loads in order to reduce the effect of offset voltage error caused because of device mismatch. Fig. 2 shows the block diagram of preamplifier based comparator. The operation of

this circuit is that the preamplifier stage amplifies the input signal and the amplified input is then fed into the latch stage using transmission gates.
The preamplifier stage isolates the input of comparator from the switching noise originating from the positive feedback stage. The input referred latch offset voltage is also reduced by the preamplifier stage. The transistor's sizes are set according to the differential amplifier trans-conductance and the input capacitance. The positive feedback latch stage determines which of the given two inputs is larger and therefore amplifies the difference.

The final component of the comparator, output buffer, converts the output of the latch stage into full scale digital level output i.e. to either logic 0 or logic 1. It is mandatory that the buffer has a differential input signal and does not possess any slew-rate limitations. The output buffer circuit is comprised of a self-biased differential amplifier followed by an inverter. The inverter stage provides additional gain and isolates any load capacitance from the amplifier stage [9]. The merit of preamplifier based comparator is its high speed and low value of offset voltage. However, the demerit is that it consumes huge static power.

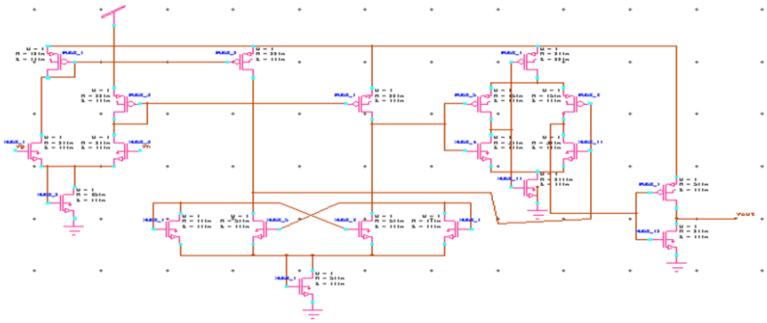

Fig 2. Schematic of preamplifier based comparator

3.2 Latch Type Voltage Sense Amplifier

Fig 3.shows the circuit diagram of latch type voltage sense amplifier [1]. It has two phases: the reset phase and the evaluation phase. During reset phase when clock is low, the output node of the comparator is reset to V_{DD} through the transistor M10 and M11. During evaluation phase when clock is high, transistor M1 turns on and the input transistors M2 and M3 starts discharging from V_{DD} to ground. When any of the node voltages falls to$V_{GS} - V_{TP}$, PMOS transistors of the inverters turns on and further improves the positive feedback. In this manner a small input voltage difference is converted to large full scale output.

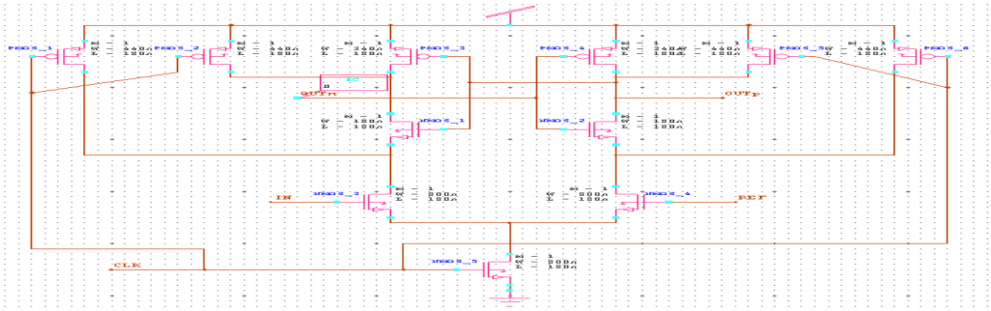

Fig 3.Schematic of dynamic latch sense amplifier

3.3 Preamplifier Dynamic Latch Comparator

Fig.4 shows the circuit diagram of preamplifier dynamic latch comparator. The preamplifier used here is self-biased fully differential circuit with active loads in order to reduce the effect of offset voltage error caused because of device mismatch. It should also have wide bandwidth and small gain to achieve high speed. It also decreases the disturbance due to kick back noise.
The dynamic latch stage consists of two cross-coupled pair of NMOS and PMOS transistors. These transistors are connected to ground through a clock enabled transistor. The use of combination of NMOS and PMOS transistors reduces the time constant upto 25% as compared to single regeneration counterpart. In order to meet the requirement of high speed and low parasitic capacitance the transistor should be small in size.

The latch can be categorized in two ways: static latch comparators or dynamic latch comparators [4]. The dynamic latch comparator uses two cross coupled CMOS inverters for regeneration. The circuit is set either in active mode or in standby mode with the help of a clock [2]. The advantage of this comparator is that it achieves higher speed without limitation of quiescent point. However, if there exists a direct connection between the output nodes of preamplifier and the regeneration nodes of the latch, kickback noise is produced. This noise results in voltage spikes at the voltage differential input signal. Therefore, transmission gate is used in between preamplifier and latch stage in order to control the signal path and provide high gain to the output signal.

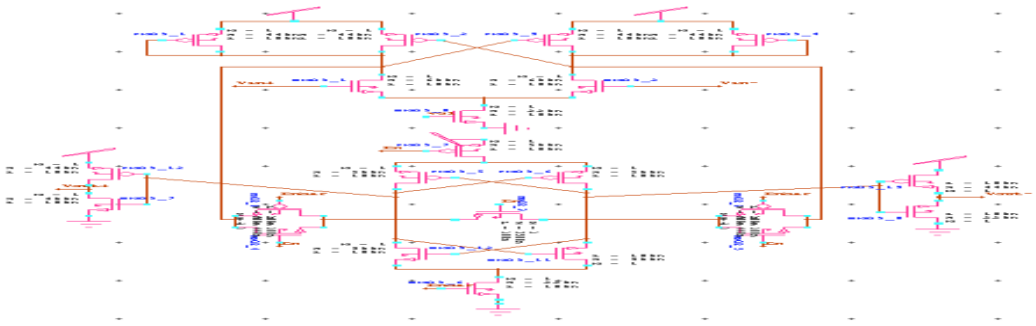

Fig 4. Schematic of preamplifier dynamic latch comparator

During reset phase when clock signal en is high, the comparator resets through the transistor M13. During regenerative phase when clock signal en is low the circuit is in comparison phase. The transistors M8 and M4 turn on. This connects the comparator to the voltage supply and to the ground and thus transmission starts.

3.4 Dynamic Latch Comparator With Inverter Buffer

Fig 5 shows the schematic of dynamic latch comparator with inverter buffer. The transistors M1, M9 and M2, M7 form the pair of inverters. The output of inverters are connected to the inputs of the other in order to form feedback.

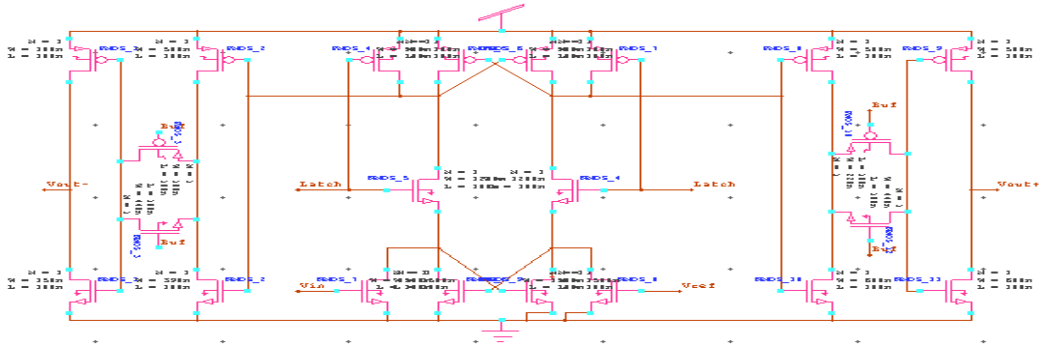

Fig 5. Schematic of dynamic latch comparator with inverter buffer

During the precharge phase, when the latch signal L_{th} is low, the transistors M5 and M8 are turned off and the transistors M1, M2 are isolated from M9 and M7. This precharges the output node to digital '1' through the transistors M3 and M4. During this phase, when the latch signal L_{th} is high, the transistors M5 and M8 are turned on and the voltage at the drain of transistors M1 and M2 starts discharging through the positive rail. When the input signal is larger than the reference signal, the voltage at drain of transistor M1 will drop faster than the output node. As soon as the input reaches $V_{GS} - V_{TN}$, transistor M2 turns on and triggers the regenerative feedback.

The demerit of dynamic latch comparator is the offset error caused due to transistor mismatch [6] and unbalanced charge residue [8]. The operation of this comparator is slow if the voltage is in the small signal range. The comparator has lower speed if a large capacitive load is used at the output.

The output of the latch stage is converted into full scale digital level output i.e. either logic 0 or logic 1 by the inverter buffer. The inverter stage provides additional gain and isolates any load capacitance from the amplifier stage [9]. The timing signal latch, L_{th} and the buffer signal, clk, must be designed carefully to avoid error and to correctly represent the relationship between input and the reference.

4. PROPOSED WORK

The proposed circuit structure is composed of two stage: a preamplifier stage and a latch stage. The circuit uses a clk and $clkb$ signal to set the circuit either in active mode or in stand-by mode. The P-logic block and N-logic block are connected in active mode. The comparator first samples the input and then this sampled input is compared to the reference, however, the output is not available at this point of time. During stand-by mode, the P-logic and N-logic are disconnected and the output reflects the last decision of the input stage. This comparator is insensitive to noise because once the decision is made, the inputs are effectively disconnected from the output by the latch stage.

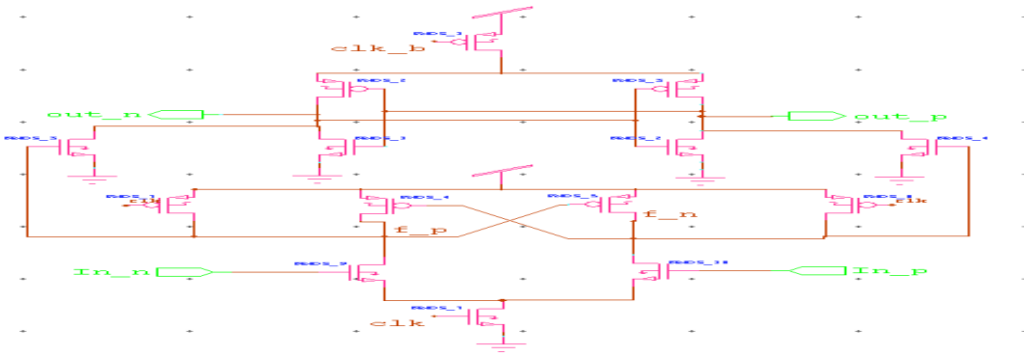

Fig 6.Schematic of proposed comparator

During the reset phase when clock is low, transistor M1 is turned off and transistors, M5 and M4 are turned on. This causes charging of nodes f_p and f_n. These charged nodes, f_p and f_n turns on the transitors, M8 and M9. Transistors, M8and M9 provide a path through which discharging of

output nodes out_p and out_n takes place. At the same time, the transistor, M10 is turned off and the latch is disconnected from V_{DD} and thus, it provides an easy way to discharge to the ground. During the evaluation phase when clock goes high, transistor M1 turns on and nodes f_p and f_n start to discharge at different rates. As soon as, any of these two nodes reaches below $V_{GS} - V_{TP}$ it forces the other node to charge to V_{DD} through transistors, M6 and M7. The potential of these nodes drive the transistors, M8 and M9. As potential of f_p and f_n starts reducing due to discharging, these transistors (M8 and M9) start turning off. Among transistors M8 and M9 whichever turns off first, the node corresponding to that transistor will go high as transistor M10 and PMOS devices of latch are already on.

The merit of this new comparator is that it operates at lower supply voltage and have stable offset voltage and also provides higher speed over wide range of common mode voltage. However, since this comparator requires both *clk* and $clkb$ signal, there must be accurate timing relationship between the two signals for optimal operation.

5. SIMULATION RESULTS

The different types of comparators and the proposed dynamic latch comparator circuit are designed simulated in Tanner EDA suite using 180 nm CMOS technology and 1V power supply voltage. Table 1.shows the comparison of power and delay of different types of comparators. Fig. 7, 8, 9, 10 and 11 show the transient responses of various comparators described above. It demonstrates that the new comparator is able to achieve higher speed with delay of 60.29 picoseconds and also consumes lower power of 0.03968 mill watts which is higher in terms of speed and is lower in terms of power consumption than the other conventional latched comparator.

Table 1.Comparison of different comparators

Comparators types	**Power** (milliwatt)	**Delay** (picosecond)
Preamplifier based Comparator	0.39768	500
Latch type Voltage Sense Amplifier	0.22013	71.026
Preamplifier based Dynamic Latch Comparator	0.2587	75.659
Dynamic Latch Comparator with inverter buffer	0.11277	76.026
Proposed comparator	0.03968	60.29

Fig 11. shows the output and input waveforms of the proposed circuit of dynamic latch comparator. The input and reference voltages are compared. When Vin > Vref then the value at output is high and when Vin<Vref then the value at output is low.

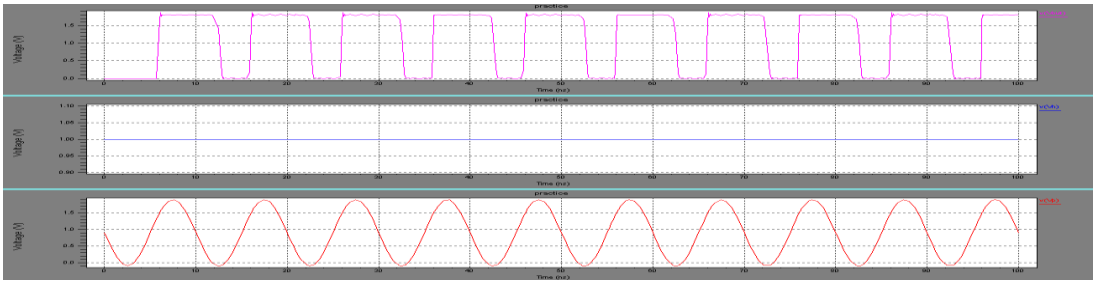

Fig 7.Transient response of preamplifier based comparator

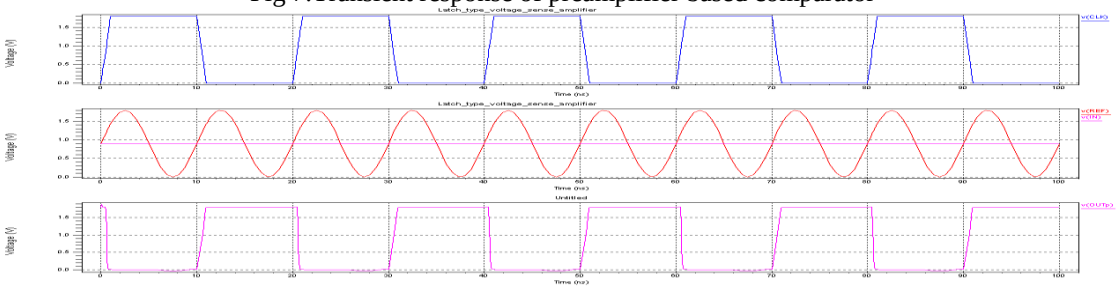

Fig 8. Transient analysis of dynamic latch sense amplifier

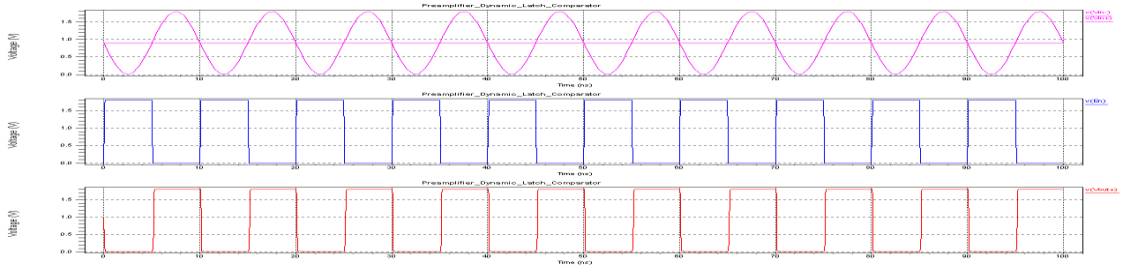

Fig 9.Transient analysis of preamplifier dynamic latch comparator

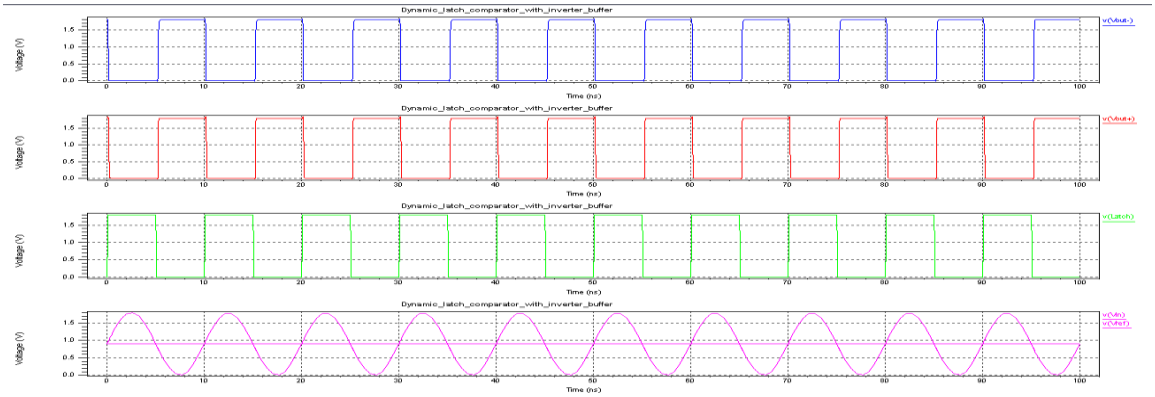

Fig 10. Transient analysis of dynamic latch comparator with inverter buffer

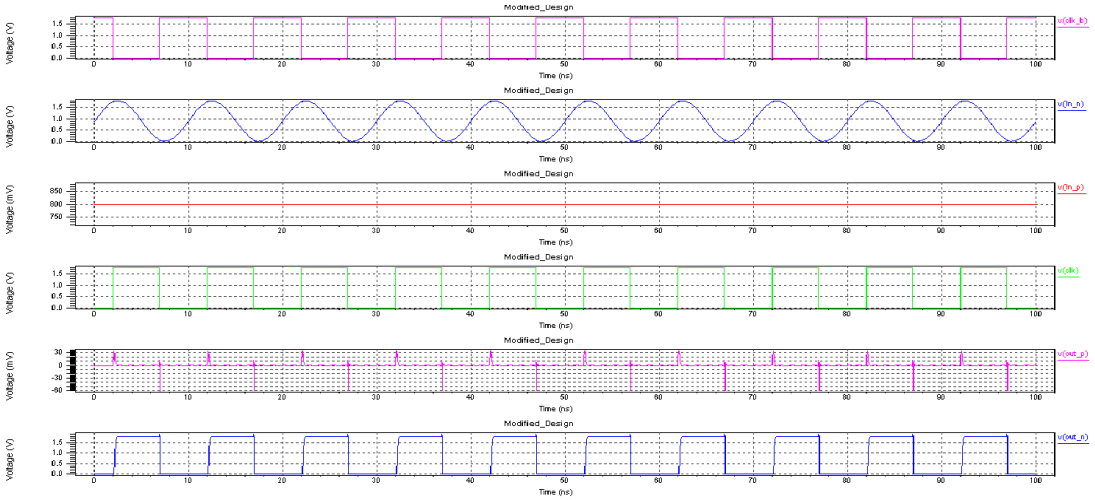

Fig 11.Transient response of proposed comparator

6. CONCLUSION

In this paper, a CMOS dynamic latch comparator with higher speed and lower power consumption is proposed. From the simulation results, it has power consumption of 0.03968 mill watts and delay of 60.29 picoseconds. Thus, this comparator can be well used in various types of analog-to-digital converters demanding higher speed along with lower power consumption.

7. REFERENCES

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