DESIGN OF LOW POWER OPERATIONAL TRANSCONDUCTANCE AMPLIFIER FOR BIOMEDICAL APPLICATIONS

Sarin Mythry[1] A.Gayathri[2], Saieemah Farheen[3], N.Jeenath[4], M.Sowmya[5], P.Sahith[6]

[1,2]Faculty, [3,4,5,6]Graduate scholars
Department of Electronics and Communication Engineering,
Christu Jyothi Institute of Technology and science,
Yeshwanthapur, Jangaon, Warangal Dist, Telangana State, India.

ABSTRACT

This paper presents the design of folded cascode operational transconductance amplifier (OTA). This design has been implemented in 0.18um CMOS Technology using Cadence. Spectre simulation shows that the OTA has flat gain of 47dB from 1Hz to 100 KHz frequency, indicating stability of OTA, noise ranges as 22.49769nV/$\sqrt{Hz}$ at 10Hz to 66.89128fV/$\sqrt{Hz}$ at 1MHz and average power as 0.770mW. In this paper, we will be studying the design concepts, analysis of operational transconductance amplifier which is used for recording the bio signals. This paper plays a key role in real time applications for equipment designing of ECG, EEG, EMG, ENG devices. It is also used in recording and also for treatment of Paralysis, Epilepsy, Neuro diseases etc.,

KEYWORDS

Folded cascode, Operational Transconductance amplifier (OTA), Cadence.

1. INTRODUCTION

By the advancement in Biomedical engineering and neuroscience it became easy to extract control signals from individual and communicate their intentions through computers or prostheses. Thus bio signals can be interfaced to neural interface microsystems and monitor a large group of neurons. But the channel faced by such microsystem is low power constraints, small form factor while providing high resolution.

In such systems Operational Transconductance amplifier plays a very role. They are the main building blocks of analog design but the problem is they consume more power. Basically OTA is an Operational amplifier (op amp) without any buffer. OTA is voltage controlled current source(VCCS) while op amp is voltage controlled voltage source(VCVS).OTA has a differential amplifier at the input. The main purpose of OTA is it provides current proportional to an input voltage difference. The main parameter of OTA is Transconductance i.e., the ratio of output current to input voltage. A simple first-order small signal model for an OTA is shown in Fig. 5.1. The amplifier's transconductance is G_{ma} and its frequency response in Fig. 5.1is given simply by $G_{ma}Z_L$. More over they are widely used because of simple design.

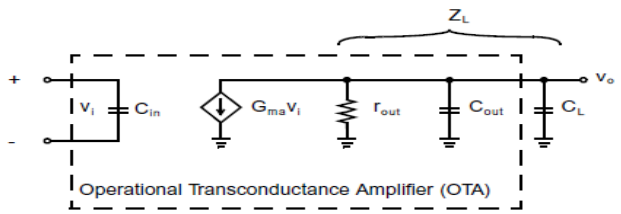

Figure 1.First-order model of an operational transconductance amplifier (OTA) driving a capacitive load.

There are many types of OTAs among which conventional OTAs are: Two stage OTA, folded cascode OTA, Telescopic OTA, Gain Boosted OTA and other OTAs are miller OTA, Current mirror OTA and so on.In this paper a folded cascode OTA is designed to satisfy flat gain and low power.

2. CIRCUIT IMPLEMENTATION

2.1 Design of Folded cascode Operational Transconductance amplifier

In this design we have used differential-input single-ended output folded cascode design. We have used here current mirrors that provide wide swing current mirrors and they are used as they provide High output impedance maximizing the DC gain Of OTA.

The basic idea of folded cascode OTA is to apply cascode transistors to the input differential pair but the transistors used are of opposite type to that of input. In our design we have used differential transistors Q_1 and Q_2 as n-channel transistors and cascode transistors Q_5 and Q_6 as p-channel. This opposite type of transistors provide single gain stage amplifier same Bias voltage at output as that of input signals. Even though the folded cascode is single stage amplifier it has high gain. This high gain is due to the product of input Transconductance and output impedance. The high output impedance is due to cascode techniques used. The shown differential-to-single-ended conversion is realized by the wide-swing current mirror composed of Q_7, Q_8, Q_9, and Q_{10}.

An important addition of the folded-cascode OTA used is the inclusion of two extra transistors, Q_{12} and Q_{13}. They serve two purposes. One is to increase the slew-rate performance of the OTA .During times of slew-rate limiting, these transistors prevent the drain voltages of Q_1 and Q_2 from having large transients where they change from their small-signal voltages to voltages very close to the negative power-supply voltage. Thus the inclusion of Q_{12} and Q_{13} allows the OTA to recover more quickly following a slew-rate condition.

The main purpose of the diode-connected transistors, Q_{12} and Q_{13} included is to clamp the drain voltages of Q_1 or Q_2 so they don't change as much during slew-rate limiting. A second, more subtle effect dynamically increases the bias currents of both Q_3 and Q_4 during times of slew-rate limiting. This increased bias current results in a larger maximum current available for charging or discharging the load capacitance.

Here compensation is provide by the load capacitor C_L, and realizes dominant-pole compensation. In applications where the load capacitance is very small, it is necessary to add additional compensation capacitance in parallel with the load to guarantee stability. If lead compensation is desired, a resistor can be placed in series with C_L.

The folded cascode opamp is a transconductance amplifier whose frequency response is dominated by the output pole at $1/R_{out}C_{L.}$

The bias currents for the input differential-pair transistors are equal to $I_{bias2}/2$. The bias current of one of the p-channel cascode transistors, Q_5 or Q_6 , and hence the transistors in the output-summing current mirror as well, is equal to the drain current of Q_3 or Q_4 minus $I_{bias2}/2$. This drain current is established by I_{bias1} and the ratio of,$(W/L)_3$ or$(W/L)_4$, to $(W/L)_{11}$. Since the bias current of one of the cascode transistors is derived by a current Subtraction, for it to be accurately established, it is necessary that both I_{bias1} and I_{bias2} be derived from a single bias network.

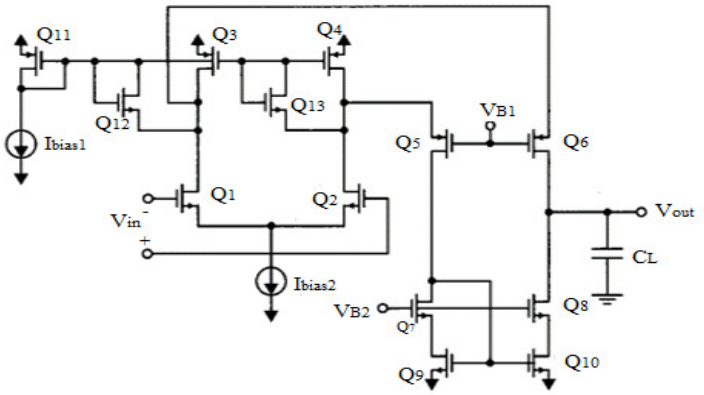

Figure 2.A folded-cascode operational transconductance amplifier.

2.2 SMALL-SIGNAL ANALYSIS

In a small-signal analysis of the folded-cascode amplifier, it is assumed that the differential output current from the drains of the differential pair, $Q_{1,}$ $Q_{2,}$ is applied to the load capacitance, C_L. Approximate small-signal transfer function for the folded-cascode opamp is given by

$$A_V = \frac{V_{out}(s)}{V_{in}(s)} = g_{m1}Z_L(s) \tag{1}$$

Here, g_{m1} is the transconductance of each of the transistors in the input differential pair, and $Z_L(s)$ is the impedance to ground seen at the output node. When the compensation is realized by the output capacitance only, we have

$$A_V = \frac{g_{m1}r_{out}(s)}{1+sr_{out}C_L} \tag{2}$$

Where r_{out} is the output impedance of OTA. This impedance is quite high, on the order of $g_m r^2_{ds}/2$ or greater if output-impedance enhancement is used.

For mid-band and high frequencies, the load capacitance dominates, and we can ignore the unity term in the denominator and thus have

$$A_V \cong \frac{g_{m1}}{sC_L} \tag{3}$$

From which the unity-gain frequency of the opamp is found to be

$$\omega_t = \frac{g_{m1}}{C_L} \tag{4}$$

With feedback, the loop unity-gain frequency is

$$\omega_t = \frac{\beta g_{m1}}{C_L} \tag{5}$$

Hence, for large load capacitances, maximizing the transconductance of the input transistors maximizes the bandwidth. One more advantage of having very large transconductance for the input devices is that the thermal noise due to this input pair is reduced. since much of the bias current in folded-cascode opamps flows through the input differential pair, these opamps often have a better thermal noise performance than other opamp designs having the same power dissipation.

Table 1.Transistors aspect ratios in (μm)

MOSFETS	**Practical values(W/L)**
NM0(Q1)	40/1.6
NM5(Q2)	40/1.6
PM2(Q3)	40/1.6
PM1(Q4)	40/1.6
PM4(Q5)	30/1.6
PM3(Q6)	30/1.6
NM1(Q7)	15/1.6
NM2(Q8)	15/1.6
NM4(Q9)	15/1.6
NM3(Q10)	15/1.6
PM0(Q11)	10/1.6
NM7(Q12)	40/1.6
NM6(Q13)	10/1.6

3.Simulation results

A folded cascode operational transconductance amplifier is designed with the design process described above and implemented in 0.18um process with 1.8 V power supply and simulated with Cadence spectre .The load capacitance is 1 pF. The parameters obtained are:

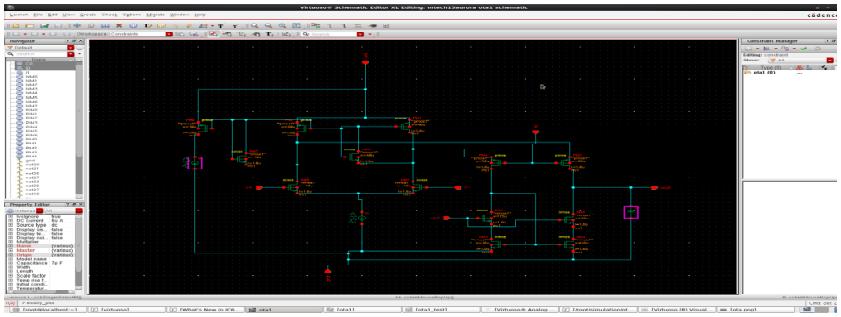

Figure 3. Folded cascode OTA schematic in cadence.

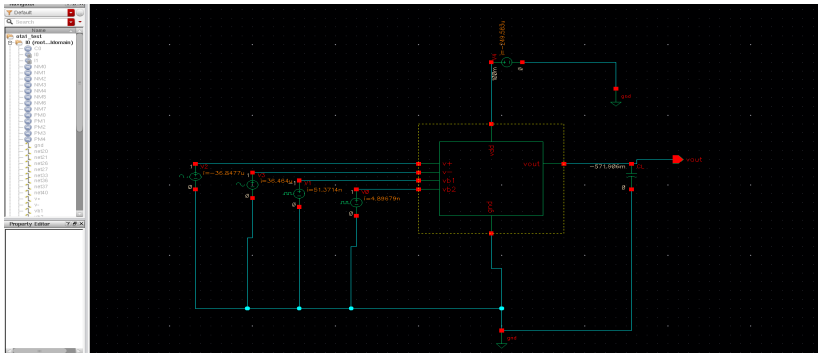

Figure 4.Symbol for Folded cascode OTA schematic.

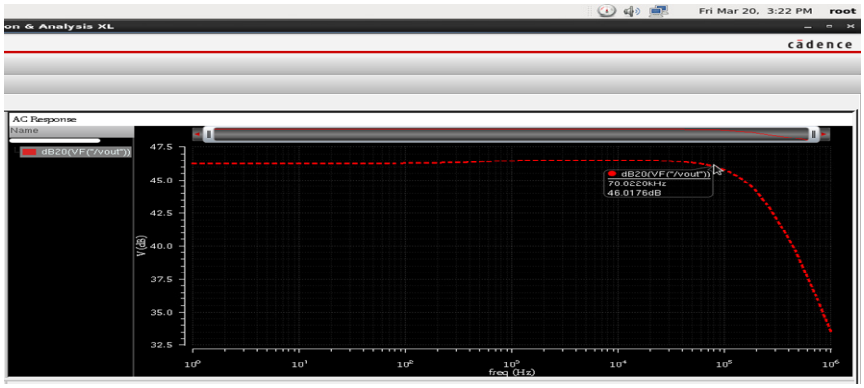

Figure 5.Gain of Folded cascode OTA.

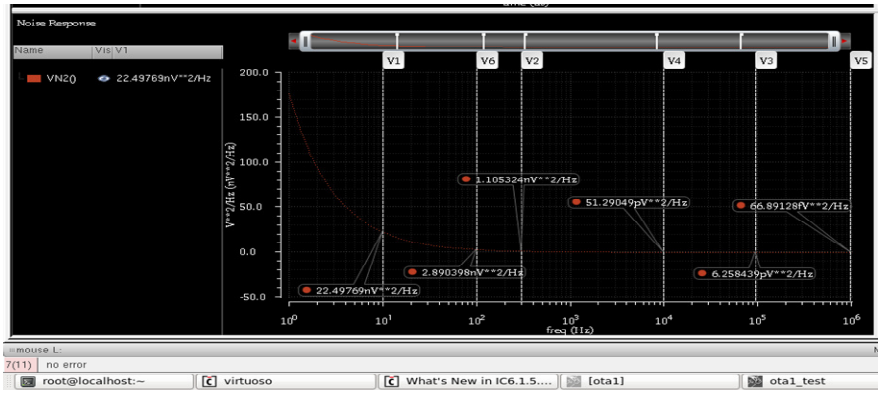

Figure 7. Noise Response of Folded cascode OTA.

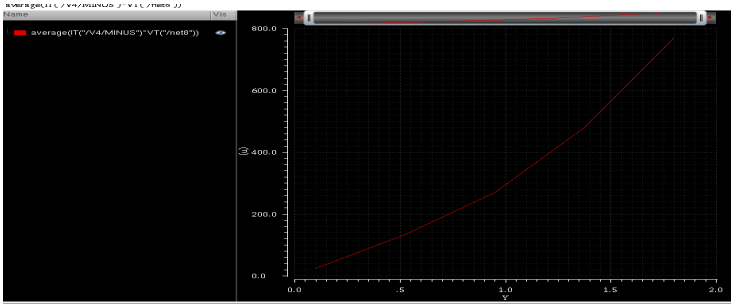

Figure 9. Average power of Folded cascode OTA.

Table 2. Simulation results

PARAMETER	RESULT
Technology	180nm
C_L	1pF
Noise	22.49769nV/$\sqrt{Hz}$ at 10Hz 2.890398nV/$\sqrt{Hz}$ at 100Hz 1.10534nV/$\sqrt{Hz}$ at 300Hz 51.29049pV/$\sqrt{Hz}$ at 10KHz 6.25439pV/$\sqrt{Hz}$ at 100KHz 66.89128fV/$\sqrt{Hz}$ at 1MHz
Flat gain	~47 dB from 1Hz to 100KHz
Supply Voltage	1.8V

4. Conclusion

The design and experimental results of folded cascode OTA has been presented, based on 0.18um CMOS process, it has good performance with a flat gain of 47 dB approximately from 1Hz to 100KHz, noise ranges as 22.49769nV/$\sqrt{Hz}$ at 10Hz to 66.89128fV/$\sqrt{Hz}$ at 1MHz and average power of 0.770mW at a power supply of 1.8 V.

ACKNOWLEGEMENT

We the students feel obliged to take this opportunity to thank our Professors **Mr.Sarin V Mythry** and **Mrs.A.Gayathri** of Christu Jyothi Institute of Technology And Science(CJITS), Jangaon, for taking keen interest and providing base ,encouragement to our project work. We would also like to thank CJITS, Jangaon for encouraging our work towards research.

REFERENCES

[1] Raghuwar Sharan Gautam,P. K. Jain,D. S. Ajnar(2012) "Design of Low Voltage Folded Cascode Operational Transconductance Amplifier with Optimum Range of Gain and GBW in 0.18µm Technology", International Journal of Engineering Research and Applications (IJERA) , Vol. 2, Issue 1, pp566-570 .

[2] Benoit Gosselin,(2011)"Recent advances in neural recording Microsystems", www.mdpi.com/journal/sensors, vol. 11, pp 4572-4597

[3] Behzad Razavi, (2002) Design of analog cmos integrated circuits, Tata McGraw-Hill Edition.

[4] Tony Chan Carusone, David A. Johns and Kenneth W. Martin, (1997) Analog integrated circuit design, John Wiley & Sons, Inc.

[5] Er. Rajni,(2011)"Design of High Gain Folded-Cascode Operational Amplifier Using 1.25 um CMOS Technology",International Journal of Scientific & Engineering Research Volume 2, Issue 11, pp1-9.

[6] M.Yousefi, A.Vatanjou, F.Nazeri, (2012) "High-Speed High-Gain CMOS OTA for SC Applications", World Academy of Science, Engineering and Technology,Vol. 6 ,pp205-208.

[7] Jalpa solanki, (2014) "Design and Implementation of High Gain, High Bandwidth CMOS Folded cascode Operational Transconductance Amplifier", IJEDR, vol. 2, issue 1, pp:532-536.