FPGA DESIGN OF CLUTTER GENERATOR FOR RADAR TESTING

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ABSTRACT

Detection of weak target echo in the presence of strong clutter is the main objective of any RADAR. To evaluate the performance of RADAR it is required to generate the clutter of various types including land and sea. This clutter is of non Gaussian distribution such as lognormal, Weibull and k-type. In this project it is proposed to develop a clutter generation algorithm of given distribution type. This process consists of random number generator with Gaussian distribution converting into a non Gaussian using ZMNL (Zero Memory Nonlinearity Transformation) technique. It also includes amplitude shaping and addition other interference signals. The complete algorithm is first simulated using Xilinx ISE 9.2i and would be implemented in VIRTEX-V FPGA.This algorithm will be used for the testing of RADAR system. Results are compared with standard results.

KEYWORDS

RADAR,Gaussian,Lognormal,Weibull,K-Type,ZMNL,FPGA,

1. INTRODUCTION

Clutter is a term used to describe any object that generates unwanted radar returns that may interfere the normal radar operations. Parasitic returns that enter the radar through the antenna's main lobe are called main lobe clutter; otherwise they are called side lobe clutter. Clutter can be classified into two main categories: surface clutter and airborne or volume clutter. Surface clutter includes trees, vegetation, ground terrain, man-made structures, and sea surface (sea clutter). Volume clutter normally has large extent (size) and includes chaff, rain, birds, and insects. Surface clutter changes from one areato another, while volume clutter may be more predictable. In this paper modeling and verification of the clutter is introduced. Clutter affects the performance of radar when detecting and tracking the targets. Hence it is very important to know the exact and feasible method of generating the clutter sequence.

Clutter echoes are random and have thermal noise-like characteristics because the individual clutter components (scatterers) have random phases and amplitudes. In many cases, the clutter signal level is much higher than the receiver noise level. Thus, the radar's ability to detect targets embedded in high clutter background depends on the Signal-to-Clutter Ratio (SCR) rather than the SNR.

There are two methods of generating the temporal correlated clutter distribution.1).Zero Memory Non Linear transformation (ZMNL) 2).Spherically Invariant Process (SIRP). The clutter is

generated by passing the correlated Gaussian random variables through a ZMNL filter.[2]. Lognormal distributed clutter can be generated by ZMNL process but not with SIRP process. In case of real time generation of the lognormal distributed clutter by ZMNL method, the DSP chip can be used. But in these days to satisfy the real time application for handling huge number of points, it takes large computation time. Hence an alternate solution is through fpga prototyping is considered in this paper.

2. MODELLING OF CLUTTER

Consider a random variable 'X' represents the amplitude of the clutter, then the probability density function of the lognormal distributed clutter is represented as follows.

$$f(x)=\begin{cases}\frac{1}{x\sqrt{2\pi\sigma^2}}\exp[-\frac{(\ln(x)-\mu)^2}{2\sigma^2}] & x>0\\ 0 & x\le 0\end{cases} \quad (1)$$

Where μ is known as scale parameter and represents the mean of ln(x) and σ is known as standard deviation of X. The mean and variance of X are given in equations below [5].

$$E[x]=\exp(\mu+\frac{\sigma^2}{2}) \quad (2)$$

$$\text{var}[x]=\exp(2\mu+2\sigma^2)-\exp(2\mu+\sigma^2) \quad (3)$$

The generation scheme for the lognormal distributed clutter by ZMNL method is shown in Fig.1. The correlation coefficient of the input and output of the system represented by ρ_{ij} and S_{ij} and the relationship between them is as shown below.

$$s_{ij}=\frac{e^{\sigma_c^2\rho_{ij}}-1}{e^{\sigma_c^2}-1} \quad (4)$$

$$\rho_{ij}=\frac{\ln[1+s_{ij}(e^{\sigma_c^2}-1)]}{\sigma_c^2} \quad (5)$$

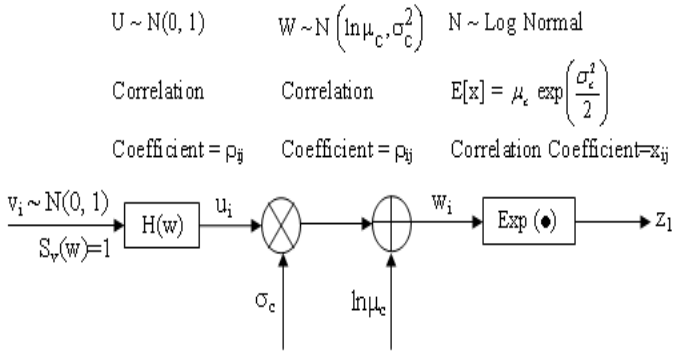

Fig.1.The scheme for the generation of Lognormal distributed clutter by ZMNL method

3. GENERATION OF LOG NORMAL CLUTTER

The Lognormal clutter generation system modeled using FPGA as shown in Fig.2, includes the random sequence generator, Gaussian sequence generator, Fast Fourier and Inverse

Fourier Transformation, matched filter and zero memory nonlinear amplitude transformation system.

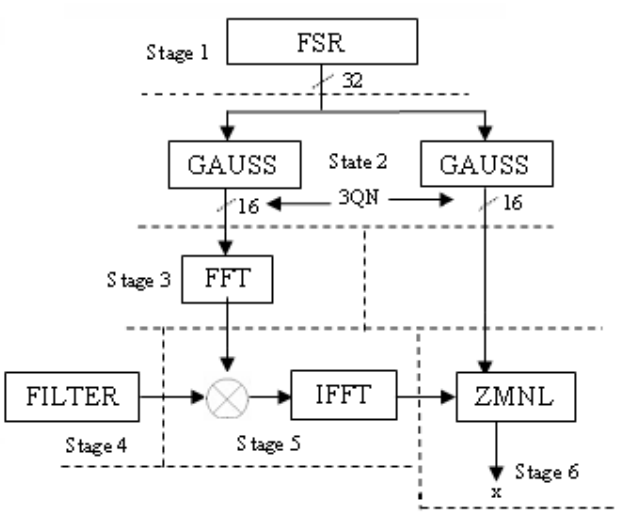

Fig.2.Block diagram of Lognormal Distributed Clutter generation

3.1. Generation of Random Numbers

The system shown above is realized in six stages. In stage one 32-bit random sequence is generated using Feed Back Shift Register (FSR). In stage two16-bit two Gaussian random sequences are generated using 32bit random sequence. Stage three to stage five is the generation of frequency filter component and its architecture is designed according to the correlated characteristic of the clutter. The final output is generated by passing the processed data and the Gaussian random sequence through the zero memory nonlinear amplitude transformation[5] filter.

Random sequence can be generated using either FSR or Tausworthe architecture as shown in Fig.3.and 4 respectively.

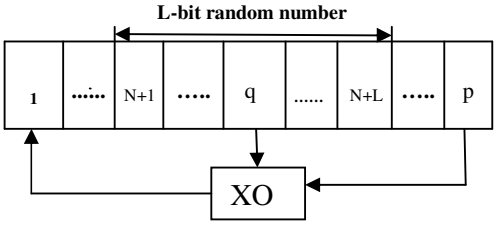

Fig.3: Random number generation using FSR

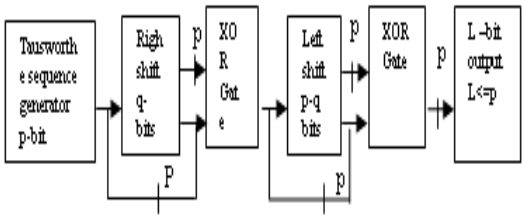

Fig.4: Improved Tausworthe generator architecture.

3.2. Generation of Gaussian Noise

Though LFSR is simple and good for different applications, to improve the randomness and the speed of sequence generation Tausworthe architecture is considered. The generation of Gaussian variable from the Gaussian is explained below. Let r_1 and $r_2$be the two 16-bit random variables in the interval [0, 1), x_1 and x_2 be the Gaussian distributed sequence with zero mean and unit variance. Then, the generated sequences are in the form of Gaussian format, which are described by equation [8].

$$\begin{cases} x_1 = \sqrt{-2\ln r_1} \times \cos(2\pi r_2) \\ x_2 = \sqrt{-2\ln r_1} \times \sin(2\pi r_2) \end{cases}$$

3.3. Design of Matched Filter

Stage 3 to stage5 explains the matched filter implementation details as shown in Fig.2. Computation of matched filter output can be illustrated in Fig. 5.

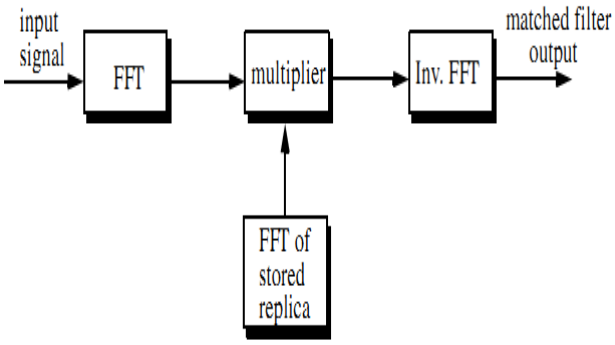

Fig.5. Block diagram of Matched Filter

Since the matched filter is a linear time invariant system, its output can be described mathematically by the convolution between its input and its impulse response.

$$FFT\{s(t) \bullet h(t)\} = S(f) \cdot H(f)$$

Where $s(t)$ is the input signal, $h(t)$ is the matched filter impulse response (replica), and the $\bullet$ operator symbolically represents convolution. And when both signals are sampled properly, the compressed signal $y(t)$ can be computed from,

$$y = FFT^{-1}\{S \cdot H\}$$

4. IMPLEMENTATION OF CLUTTER GENERATOR

HDL code for Random number generation is implemented in Virtex-V (ML501) FPGA. Hardware is designed in LABVIEW for generation of Gaussian noise. Matched filter is realized in MATLAB. ZMNL for Gaussian noise and output of matched filter which generates is implemented in LABVIEW.Fig.6 and shows the VLSI implementation flow of Tausworthe architecture.

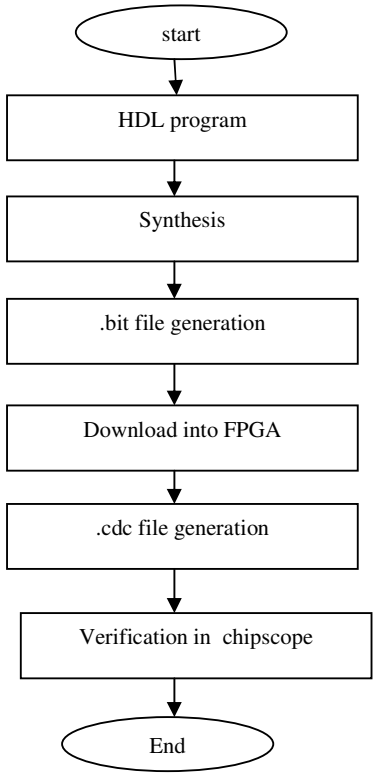

Fig.6. VLSI implementation of PRNG using Tausworthe Architecture.

HDL code is generated, simulated and synthesized .bit file is generated using VHDL. Device is configured using this bit file. By adding .cdc file, code is verified using Chipscope Pro.Fig.7, Fig.8 represent the generation of random number generator and clutter generator in LABVIEW.

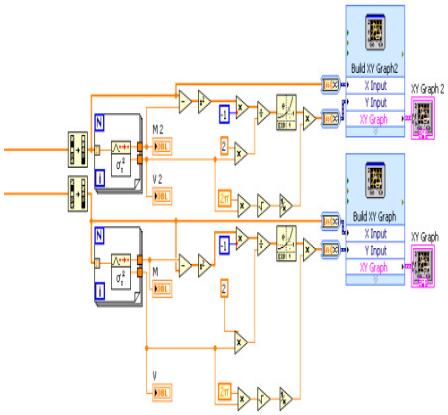

Fig.7: Generation of PRNG

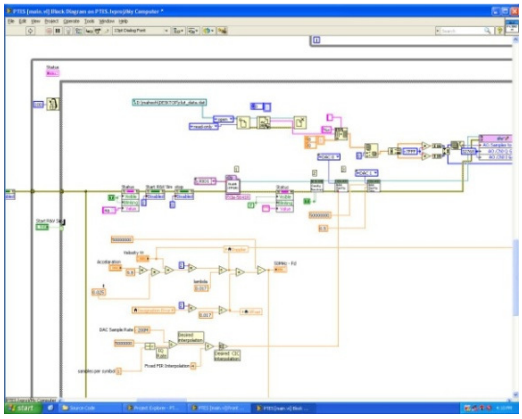

Fig.8. Implementation of Clutter Generator

5. SIMULATION RESULTS

VHDL code for random number generation is implemented on Virtex-V FPGA. CODIC IP and Chip scope Pro are used to analyze the design. Fig.9, Fig.10, Fig.11, Fig.12, Fig.13, Fig.14, Fig.15, Fig.16 represents the CORDIC IP implantation of random number, output using chipscope, PDF of Gaussian Noise, simulation result of generation of Gaussian noise using LABVIEW, Uncompressed Echo From The RADAR, Compressed Echo from the Filter, Matched Filer Time And Frequency Domain Response, Clutter generated in RADAR SEEKER.

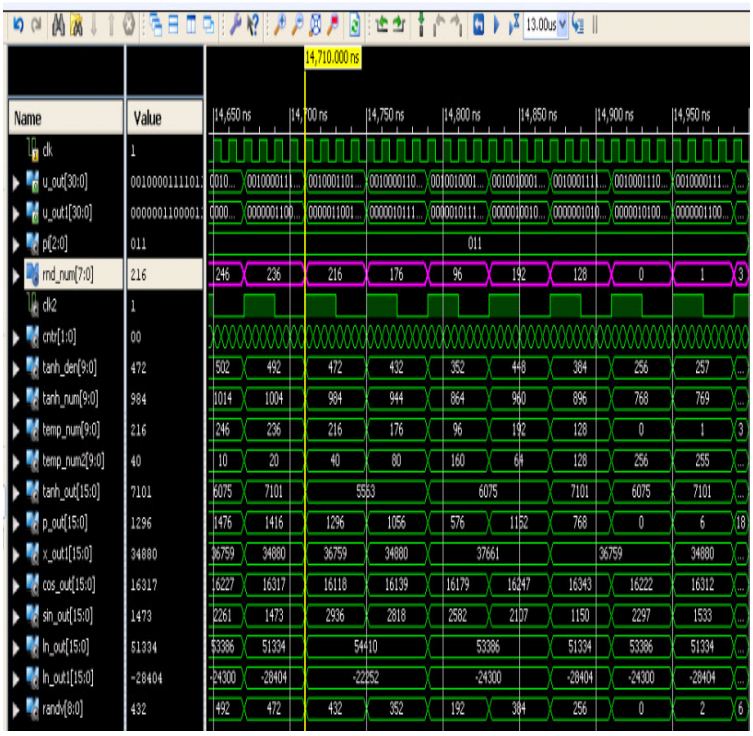

Fig.9 : Simulation result of Random number using CORDIC IP(9)

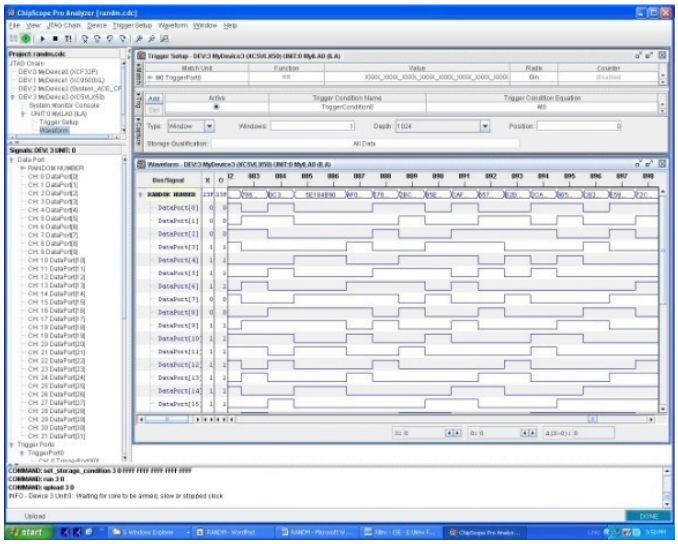

Fig.10: Simulation result of Random number using Chipscope Pro.

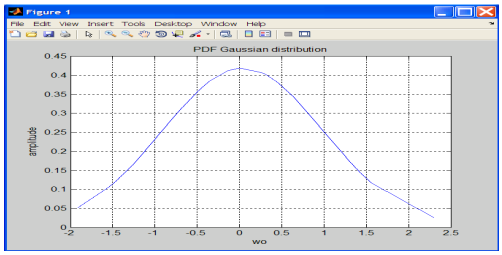

Fig.11. PDF of Gaussian Noise(10)

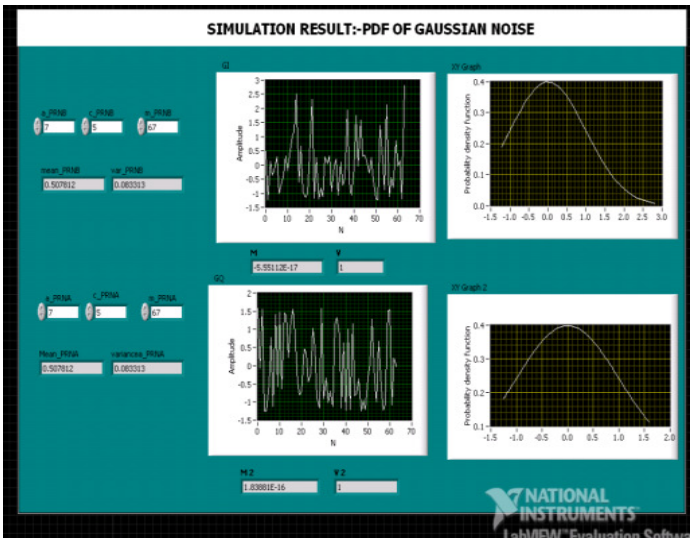

Fig.12: Simulation result of PDF of Gaussian Noise.(10)

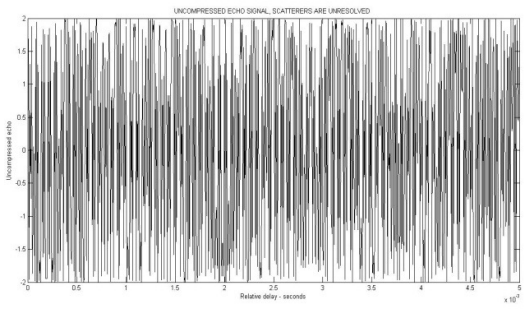

Fig.13: Uncompressed Echo from the RADAR.

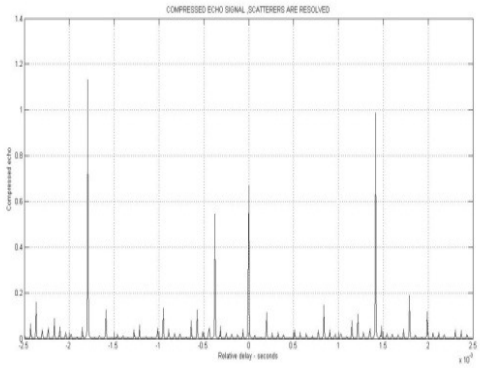

Fig.14. Compressed echo after passing through filter

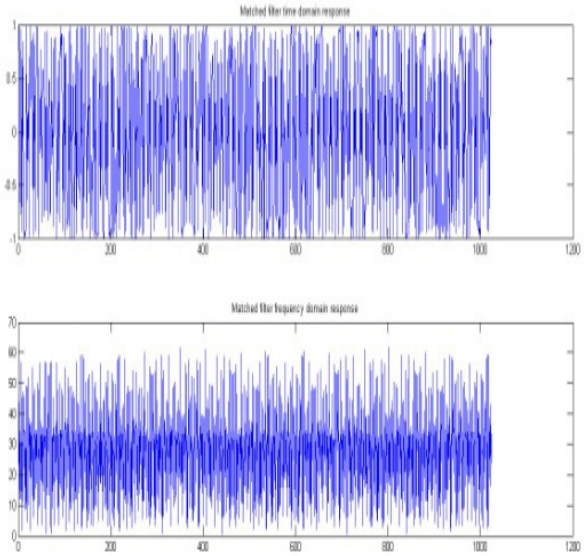

Fig.15. Matched filter time and Frequency Response

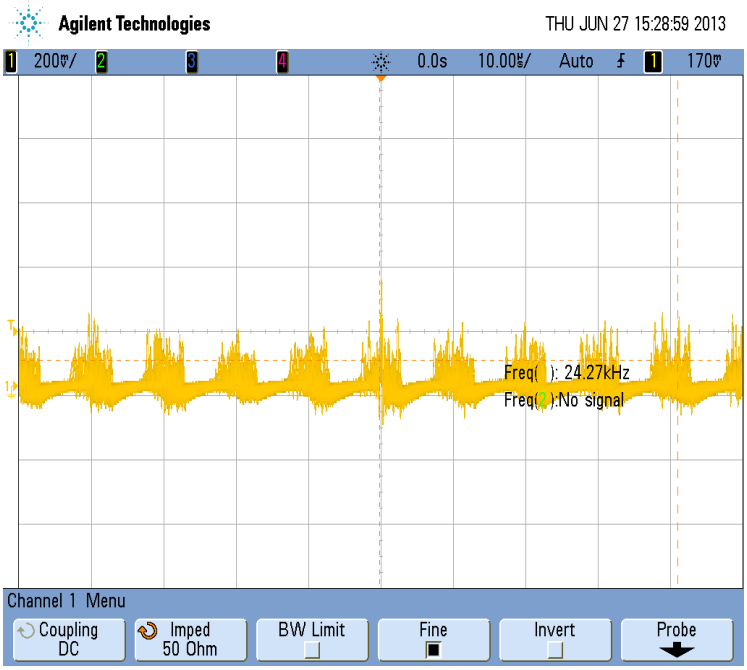

Fig.16: Generated Clutter from RADAR SEEKER.

If we take samples from the generated clutter and plot on MATLAB it takes the shape of Lognormal PDF.

It is shown in Fig.17

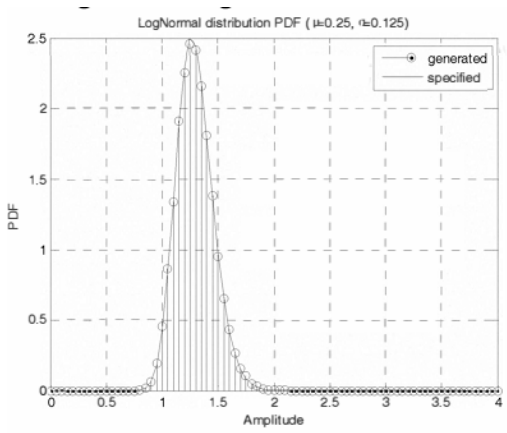

Fig.17: plot taken from Various Samples.

6. CONCLUSIONS

In this study hardware is proposed to generate lognormal distributed clutter. Improved Tauswothe architecture, boxmuller algorithm,CORDIC IP, Chipscope pro are used to generate the random numbers. MATLAB is used to design the Matched filter. LABVIEW is used to design Gaussian

noise generator, clutter generator. RADAR Seeker is tested using this result is used to tested using this result. It can be used in echo simulator, for range and velocity simulations. It is shown in Fig.18

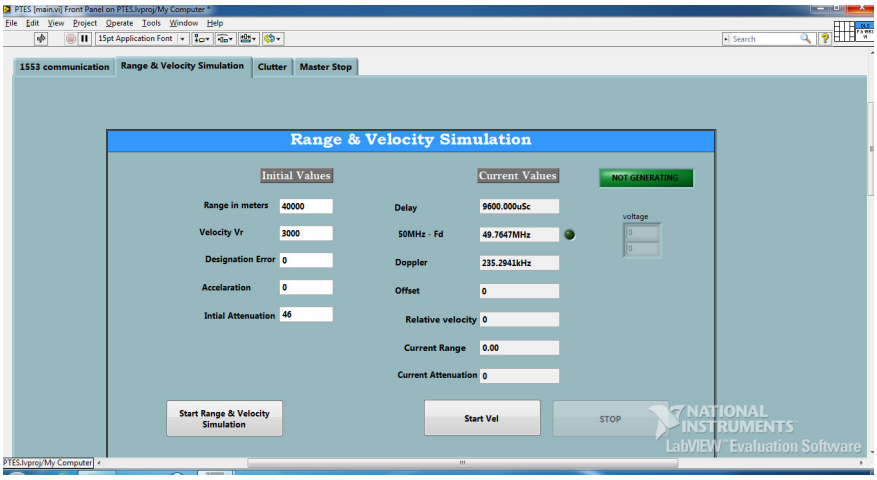

Fig.18: Using clutter Generator for range and velocity Simulation.

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