MULTI-CHANNEL FREQUENCY SYNTHESIZER BASED ON PHASE ACCUMULATOR

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ABSTRACT

This paper reports a novel architecture for multi-channel sine and square wave synthesizer. A phase accumulator is the core of multi-channel synthesizer. The phase accumulator's output is multiplexed on the output channels and held by each channel latch. It is considered the MSB of the phase accumulator as the square wave synthesizer output. According to the proposed architecture, a 4-channel square wave synthesizer is designed, simulated and implemented. Spartan-Xc3s400 from Xilinx-FPGA family is used to physically implementation. The system consumes 161 mW@40 MHz. The frequency resolution of the square wave synthesizer is 0.3 Hz in a range of 0-5 MHz. Finally, a novel architecture is proposed to produce sine from square wave and using designed 4-channel square wave synthesizer a 2-channel sine wave synthesizer is designed and simulate.

KEYWORDS

FPGA, Frequency synthesize, Multi-channel, Sine wave, Square wave

INTRODUCTION

Modern microelectronics has led to improve communication systems by integrating large-scaled circuits in to a small area chip. Now, we can integrate many communication blocks in to a single chip. They consist of analog and digital signal processing units. Frequency synthesizers that produce sine or square waves with tuneable frequencies are one of the most important devices in communication systems.

All amplitude modulators, demodulators and signal processor units need to frequency synthesizers. Frequency resolution, power dissipation, area on chip, frequency switching speed, phase noise and spectrum purity are some parameters to evaluate a frequency synthesizer [1]. Direct analog (DA), phase look locked (PLL) and direct digital frequency synthesizer (DDS) are common frequency synthesizers.

In DA, a group of reference frequencies are mixed, added or divided to synthesize the required frequencies [2]. A PLL is a feedback mechanism locking its output frequency to a reference. Recently, by improving high-speed digital integrated circuits, direct digital frequency synthesizers (DDSs) have been developed. High frequency resolution and frequency switching with continence-phase are two advantages of DDSs [3]. In some applications, we need more than one channel tuneable frequency synthesizer and by current methods, DA, PLL and DDS, it is needed to add additional reference clock pulse or components that they increase power dissipation and area occupation on chip.

In this paper, first, we introduce a phase accumulator capacity to generate square wave with tuneable frequency. Then, a multi-channel square wave synthesizer employing single reference pulse clock is designed and implement. Based on the proposed system, a 4-channel square wave synthesizer is physically implemented on an FPGA chip. Finally, we employ the square wave synthesizer to design a two-channel sine wave synthesizer. In the proposed sine synthesizer, three phase shifted square waves are added together to generate a sine wave. In section 2, the proposed system is described and the implementation of a 4-channel frequency synthesizer is shown. Using this idea, we introduce a 2-channel sine wave synthesizer in section 3 and conclude the paper in section 4.

1. MULTI-CHANNEL SQUARE WAVE FREQUENCY SYNTHESIZER

Phase accumulator is a digital device that accumulates the input word by each clock pulse. It contains an adder by a followed latch. Figure 1 shows the phase accumulator structure. The operation of a phase accumulator is given by

$$s(n)=s(n-1)+w \quad (1)$$

Where s(n) is the output in n^{th} clock pulse and w is the control word. If we consider the MSB of phase accumulator as the output, the average frequency of the square wave is

$$F_{avg} = w \times F_{clk}/2^N \quad (2)$$

Where F_{clk} is the clock frequency and N is the phase accumulator's length. In DDSs there is a processor that maps the phase accumulator output to sine amplitude. Sometimes, it is needed just a tunable square wave and it can be used the MSB of phase accumulator and the frequency is tuned by the control word.

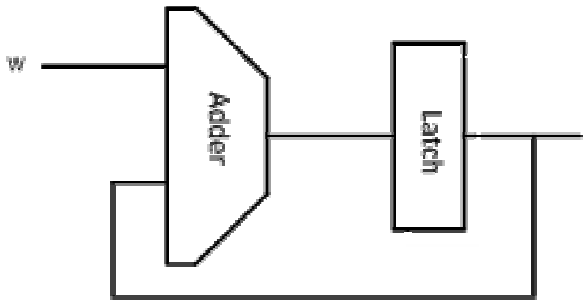

Figure 1. The phase accumulator structure

In some applications, we need more than one channel tuneable square wave. By using above architecture, it can be employed per-channel phase accumulator or single phase accumulator as the synthesizer core with additional block to produce multi-channel square wave. Figure 2 shows the proposed system. In this system, controlling words identifying each channel frequency are multiplexed on to the phase accumulator's input. The phase accumulator's output is demultiplexed on to channels, sequentially and a per- channel latch holds the last number and they are multiplexed on to the second input of the phase accumulator adder. A counter controls two multiplexers and the demultiplexer and they are synchronized together. However, to keep the frequency resolution and frequency range constant we must increase the frequency of clock according to the channel counts.

To evaluate this architecture, it was designed and simulated one, 2, 4 and 8-channel frequency synthesizer and derived power dissipation and area occupation for each of them. Spartan-Xc3s400 from XILINX-FPGA family was used in simulation process and also it was employed a 25-bit adder for the phase accumulator. Table 1 lists measured power dissipation and element counts for

each configuration. Referring to this table, the total power dissipation is just increased from 158 mW for single-channel synthesizer to 162 mW for 8-channel synthesizer and it is a noticeable power saving compared to usage each-channel phase accumulator. Besides, the system has just single reference clock pulse and this leads to a synchronic drift all channels by drifting reference clock

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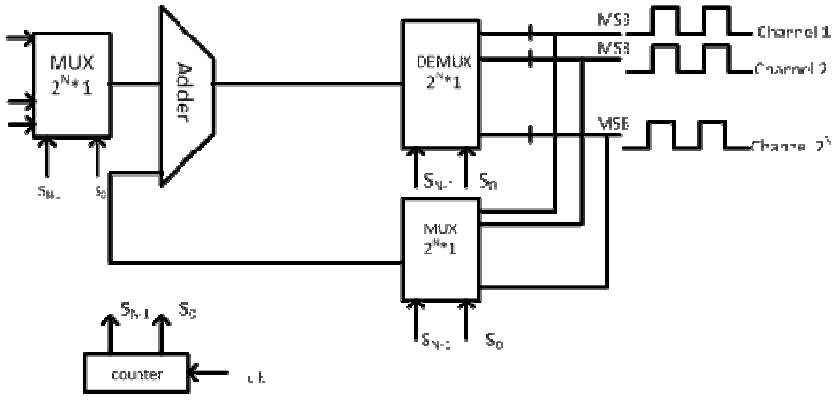

Figure 2. The proposed architecture for multi-channel synthesizer

Table 1. Measured parameter for multi-channel frequency synthesizer

Channel count	Number of Slice Flip Flops	Number of 4 input LUTs	Total power (mW)	Clock Frequency (MHz)
1	25	26	158.63	10
2	55	110	158.98	20
4	111	384	160.1	40
8	220	699	162.1	80

Figure 3 shows per-channel total number of flip-flops and LUT as the total element counts and power dissipation production. It can be a suitable parameter to evaluate system operation. As this figure shows, per-channel power dissipation and the element counts increase up to 4 channel and then decrease.

A 4-channel frequency synthesizer which employs a 25-bit adder with 40MHz clock frequency was physically implemented and tested on to the mentioned FPGA type. The adder is a pipe-lined adder and consists of a pipelined 13-bit with 12-bit adder. Due to the multiplexing process, the clock frequency is shared among the four channels. Therefore, the effective clock frequency of each channel is 10 MHz and referring to Eq. (1) the frequency resolution of each channel is 0.3 Hz (10 MHz/2^{25}). Figure 4 shows a recorded channel by digital oscilloscope that is set to 156 kHz.

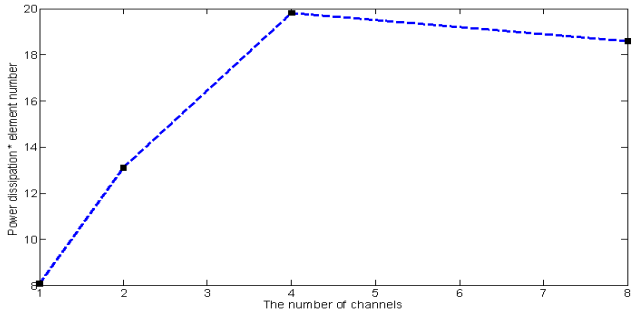

Figure 3. The power dissipation and total elements number multiplication

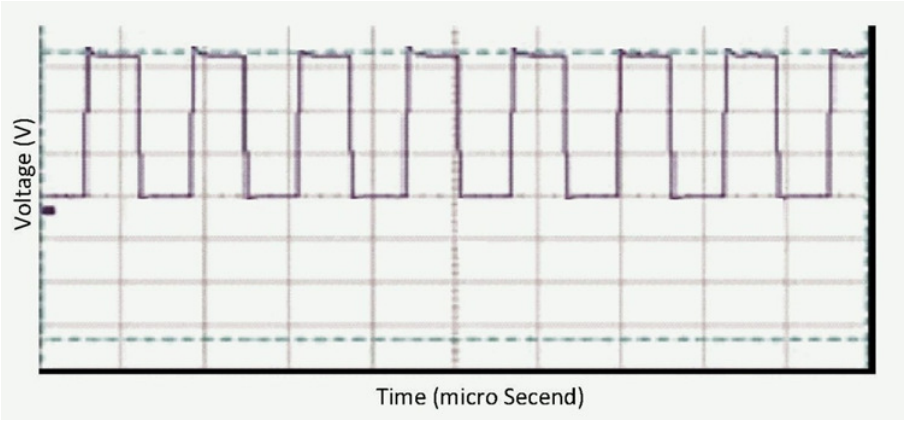

Figure 4. The output of the physically implementation of 4-channel synthesizer (time division is set to 5µs)

2.Multi-channel Sine wave synthesizer

Synthesizing sine wave is an important task in RF systems. Recently, by improving digital circuit speed, DDSs has been used widely in communication systems. But, it is needed a DDS for each channel and because of high power dissipation and area occupation of the DDSs, it is limited usage of DDS. Therefore, minimizing power and area of DDSs are two goals which they can help employing DDSs in RF systems. Removing mapping unit that maps the phase accumulator output to sine amplitude can decrease system complexity in DDSs. The proposed square wave can be changed to a sine wave synthesizer.

To synthesize sine wave by the proposed multi-channel square wave generator, the channels must be filtered to remove additional harmonic terms. However, it is needed a very sharp tuneable filter that the implementation of such filter is difficult task and needs large area on chip and power dissipation in integrated circuits. To overcome this problem, the filter order can be lowered by removing some low frequency additional harmonic terms.

Combining three square waves with -45, 0 and 45 degree phase shifted and weighted as $1:\sqrt{2}:1$, respectively, the 3rd and 5th order harmonic terms are suppressed. Removing these harmonics leads to decrease filter order to produce a pure sine wave. Figure 5 shows the proposed circuit which generates above mentioned phase shifted square waves. In this circuit, two channels are configured to produce square waves with two and four times of desired frequency. We can easily

adjust proposed multi-channel synthesizer to produce mentioned waves by the control words. Three T-flip flops with NAND gate produce mentioned phase shifted waves and add together as $1:\sqrt{2}:1$ ratio by an analog adder. Finally, a tuneable low pass filter (LPF) removes additional harmonic terms.

Using this architecture, we can directly synthesize sine wave from phase accumulator output. This synthesizer has DDS benefits that are high frequency resolution and continuous phase switching. Besides, because of not using ROM and (digital to analog converter) DAC, it has less complexity than common DDSs and is more power efficient and area occupation. In addition, we can easily synthesize sine wave more than one channel by multi-channel square wave generator.

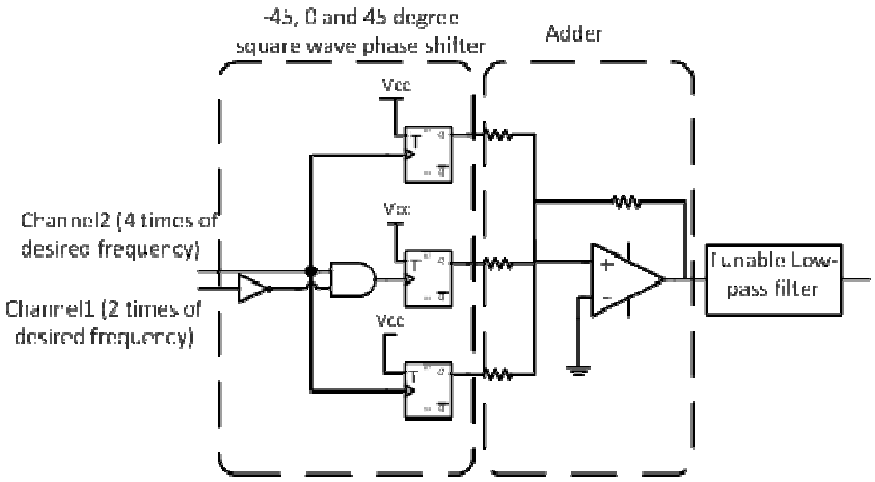

Figure 5. A novel square phase shifter to shift -45, 0 and 45 degree

To evaluate the proposed architecture, a 2-channel sine wave using designed 4-channel square wave synthesizer was designed and simulated. Figure 6 shows the designed system block diagram. We used tunable 2-order Sallen-Key low-pass filter as LPF block. A voltage controlled resistor that controlled by a digital to analog converter adjusts high-cutoff frequency in LPF. The DAC voltage is determined by control frequency words.

This synthesizer was set to generated two sine waves with 10 kHz and 100 kHz frequency. In order to these frequencies, control words were valued to 67108 and 134217 for the first channel and 6710 and 13421 for the second one, respectively. We recorded first channel signal before filtering and Figure 7 shows the spectrum of output. This synthesizer has 0.3 Hz (10 MHz/2^{25}) frequency resolution and can generate sine wave with frequency range of 0-5 MHz. To test frequency-switching behavior of it, input control words were changed to change the first channel frequency from 10 kHz to 40 kHz, quickly. Figure 8 shows the output in switching transition. As this figure shows signal frequency is changed with continues phase that this behavior is an important factor for synthesizers. The amplitude of 7^{th} harmonic term of the sine-wave is -30 dB less than the main harmonic. By increasing the order of filter the purity spectrum of sine wave will be improved. Generally, in DDS synthesizers, 10-bit resolution is employed [5]. In the proposed system, we can generate a sine-wave with suitable resolution by adjusting the order of LPF.

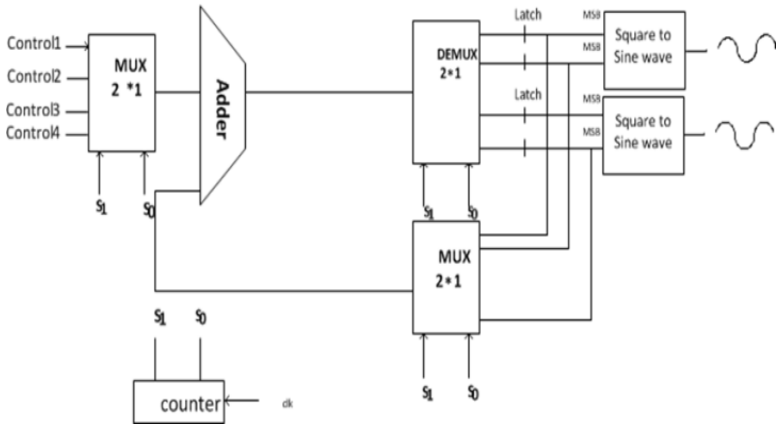

Figure 6. A 2-channel sine wave synthesizer

3.CONCLUSION

This paper presented a simple structure using a single-phase accumulator to generate multi-channel square wave. We showed that above a certain channel count it saves power dissipation and area occupation. In addition, a novel approaches employing two square wave channels to convert a square to sine wave. Although there are some approaches to convert phase samples at the output of the phase accumulator into the associated sine-amplitude samples [3-9]. In all of them it is needed a complicated mathematical operations that employing complex digital circuits. In our proposed structure we can expand channels easily and it is used a simple circuit. The proposed system is more power and are efficient than common DDSs. Finally, based on proposed method a 4-channel square wave was physically implemented and a 2-channel sine wave was designed and simulated.

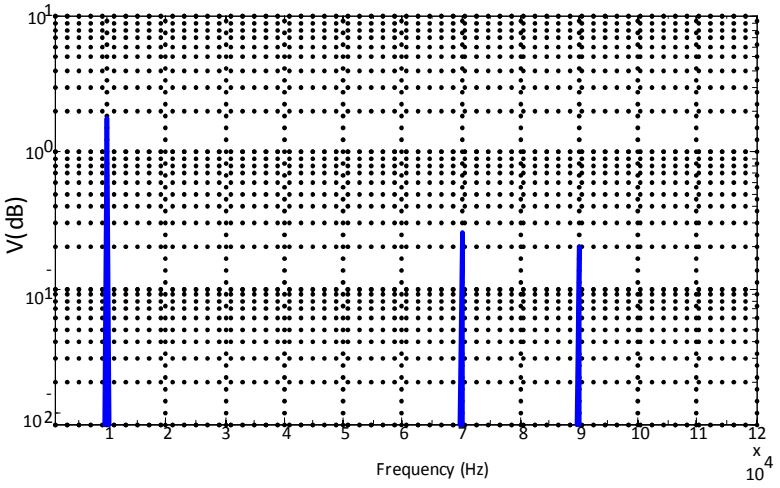

Figure 7. The spectrum of the first channel before filtering

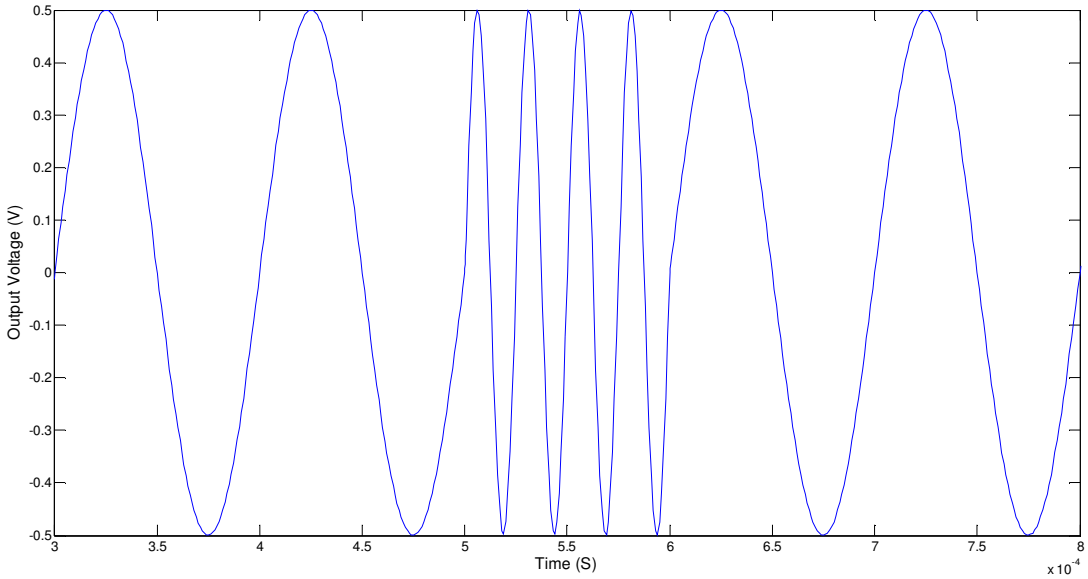

Figure 8. The first channel frequency switching behavior

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