

DESIGN AND ANALYSIS OF 2 GHz 130nm CMOS CASCODE LOW NOISE AMPLIFIER WITH INTEGRATED CIRCULARLY POLARIZED PATCH ANTENNA

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ABSTRACT

This work, illustrates the development of 2 GHz Low Noise Amplifier (LNA) interfaced with square truncated edge-fed right circularly polarized patch antenna. The LNA is simulated on Agilent ADS platform with TSMC 130nm RF CMOS process. The development of cascode amplifier and its optimization has been further exemplified. The developed LNA is tuned for 2 GHz and the performance is tuned for high stability factor of 4, Gain of 19 dB which is essential for any mobile device, Noise Figure (NF) of 1.15 dB with a P1dB point at -9 dBm. Further a truncated patch antenna with right circular polarization has been simulated on EMpro. The antenna has a gain of 6.1 dB in the azimuth plane. The simulated system can be further integrated to form the RF front end of TDD2000 LTE standard mobile device.

KEYWORDS

Cascode, LNA, 130nm, azimuth, cascode

1.INTRODUCTION

Low Noise Amplifier is used in communication system to provide basic amplification of the signal received at the antenna terminal. LNA is critical part of an RF receiving module and it defines the receiver's sensitivity. Its main function is to provide enough gain to overcome the noise of subsequent stages, while preserving voice or data quality. Its main function is to amplify extremely low signals without adding noise, thus preserving required signal to noise ratio of the system at extremely low power levels and also aid in eliminating channel interference. Conventionally, the RF front-end generally using GaAs, bipolar or BiCMOS, but due to the large power consumption, and process compatibility problems, making more difficult and not easy for integration of a wireless communication system-on-chip integrated. Due to complexity of the signals in today's digital communications, additional design considerations need to be addressed during a LNA design procedure. With the development of the RF CMOS integrated circuit technology, the MOS device size is reduced, the design of CMOS process has reached few to nm, the high frequency characteristic of the MOS device is also improved, and cutoff frequency has reached more than 200 GHz [1]. Therefore, the RF front-end IC CMOS process vast market and a good prospect is one of the hot spots in the wireless communication research.

In this paper a LNA with cascode structure for 2 GHz operation with a low noise figure of < 2dB with a port impedance of 50Ω and a Gain > 18 dB is developed. Further the developed patch antenna for 2 GHz with a considerable high gain with right circular polarization for TDD 2000 standard is simulated. The developed LNA and Antenna are interfaced and the front end is

simulated for its performance. Performance analysis of the cascade LNA and Antenna has been carried out followed by the analysis of the front end interface.

2.Cascode LNA

The classic cascode amplifier is often used with source degeneration inductor for low noise performance and high gains. Figure 1, shows the cascode amplifier for LNA which achieves low noise by increasing the noise input conjugate and match the input impedance of 50 ohms.

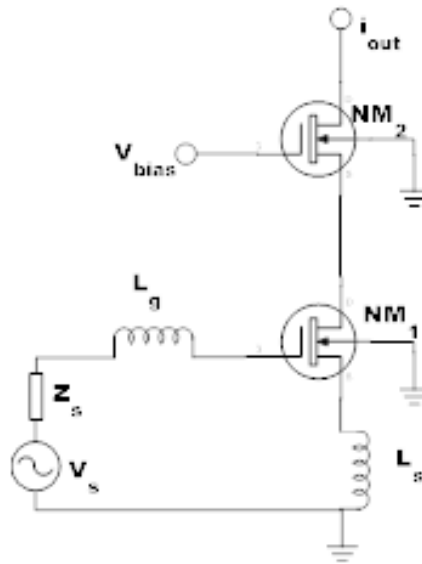


Figure 1. Cascode Amplifier

Figure 2 shows the small signal equivalent circuit, which contains the internal noise of the MOS. Since the circuit noise is primarily contributed by the decision circuit of the input stage, in order to simplify the analysis only NM1 MOS is analyzed. The NM1 the gate, drain and source parasitic resistance and parasitic capacitance between the gate-drain are also considered.

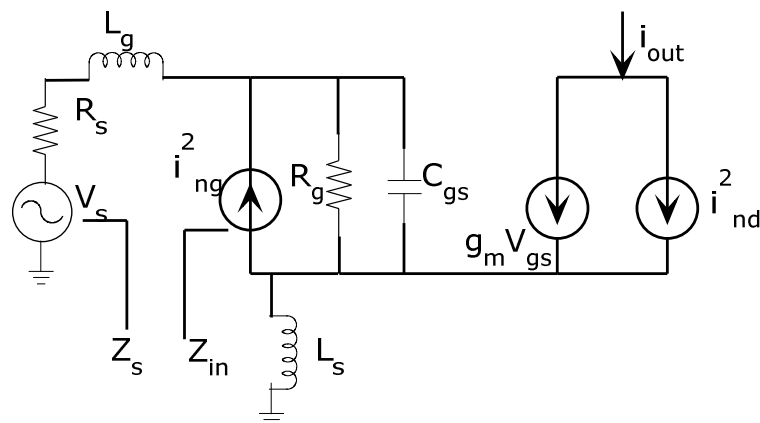


Figure 2. Equivalent Circuit of Cascode Amplifier

In Figure 2 the NM1 drain end of the channel current, thermal noise is introduced due to the non-quasi-static effect transistor gate noise, the above two kinds of noise are derived from the same kind of physical effects i.e. channel resistance thermal noise [2,3] between them there is a certain correlation, the correlation coefficient is defined in equation 1:

$$c = \frac{i_{ng} - i_{nd}^*}{\sqrt{i_{rg}^2 - i_{nd}^2}} \text{ --- (1)}$$

c is a pure imaginary number, for long channel devices. Through a series of mathematical operations, the cascode amplifier noise parameter expression is obtained in equation 2:

$$N = \frac{Y}{\alpha g_m} \text{ --- (2)}$$

Wherein, as the channel length decreases and increases, indicates the degree of deviation from the length in long channel MOS.

Under normal circumstances, the LNA's output impedance is equal to 50 ohms, while the higher gains requires a larger gate width, but this increases the power consumption of the LNA.

3. LNA Design

A complete low-noise amplifier can be divided into four parts: amplifier circuit, bias circuit, the input matching circuit and output matching circuit. The core of the amplifier circuit is the bias circuit to provide power supply. The design uses common-source common-gate circuit structure (Cascode), the bias circuit DC voltage source bias. As shown in Figure 3.

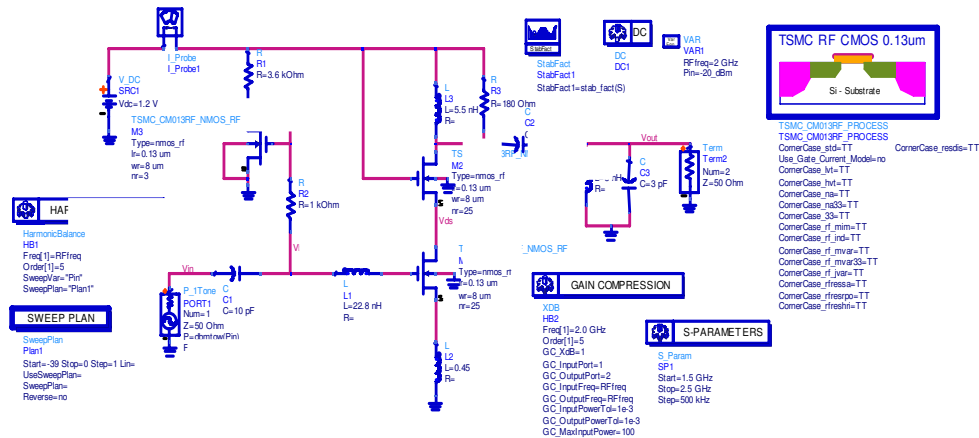


Figure 3. Simulation Circuit of 2 GHz 130nm TSMC RFCMOS Cascode LNA

M1 MOS is used in common-source amplifier configuration, as the main amplifier circuit to provide a sufficiently high enough gain. M2 MOS of the gate used reduces M1 Cgd caused by the Miller effect, in order to increase the reverse isolation characteristic of the circuit, while increasing the output impedance of the amplifier. DC bias resistance guarantee AC signal will not bias circuit DC voltage source and resistor in series to achieve the M1 MOS into the DC path.

3.1. LNA Circuit Design

1) The circuit parameters

(A) Depending on the process the required circuit parameters are calculated. [4]

The LNA is developed using TSMC _ RF _ COMS _ 0.13 μ m_V1.7 process, from the process file we infer:

$$T_{oxnrf} = 2.81e^{-9}m \quad - (3)$$

$$\mu_n = 0.0311 \frac{m^2}{Vs} \quad - (4)$$

$$V_{thn} = 0.36V \quad - (5)$$

$$C_{gs0} = 2.6e^{-10} \quad - (6)$$

From the formula:

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{3.9 * 8.8 * 10^{-14}}{2.5 * 10^{-9}} = 13.728 \frac{fF}{\mu m^2} \quad - (7)$$

(B) Calculation of optimal width W_{opt}

By power consumption constraints noise optimization theory formula

$$W_{opt} \approx \frac{3}{2\omega L C_{ox} R_s Q} \quad - (8)$$

$$Q = |c| \sqrt{\frac{5\gamma}{\delta}} \left(1 + \sqrt{1 + \frac{3}{|c|^2} \left(1 + \frac{\delta}{\gamma} \right)} \right) \approx 4 \quad - (9)$$

Considering $\omega = 2$ GHz, $R_s = 50 \Omega$, $L = 0.13 \mu m$, $Q \approx 4$

We get $W_{opt} = 200 \mu m$

(C) The bias voltage is determined according to the power requirements and the operating current of the circuit.

Considering an operating voltage of 1.2V and nominal power requirements, the drain current around 4mA is set and an overdrive voltage of 0.1V with a bias voltage of 0.4.

(D) Considering: $L_g = 22.8$ nH, $L_s = 0.45$ nH for biasing and matching the output matching network matched to 50Ω . LD, R7, C2, L7, the value of C4 most Cascode configuration of an equivalent circuit and the matching network equivalent circuit to achieve total 2GHz at the operating frequency and equivalent resistance 50 ohm output port.

(E) Noise Figure (NF2)

Can be adjusted by adjusting the total gate channel width W and LG noise figure.

(F) The stability (stabfact1)

Used by ADS parameters stabfact1 to determine whether the circuit is stable. Actual debugging and found that and by reducing LD, adjust the C5, M1 width to length ratio can be adjusted stabfact.

3.2. Simulation results

The LNA is simulated for the designed performance with matched input and output loads. Figure 4 shows the amplifier stability > 4 at 2 GHz. This signifies that the LNA is stable and in linear mode. The value of stability > 4 signifies any change in input and output impedance might not affect the stability of the system. This is also essential since an antenna is interface to the front end system.

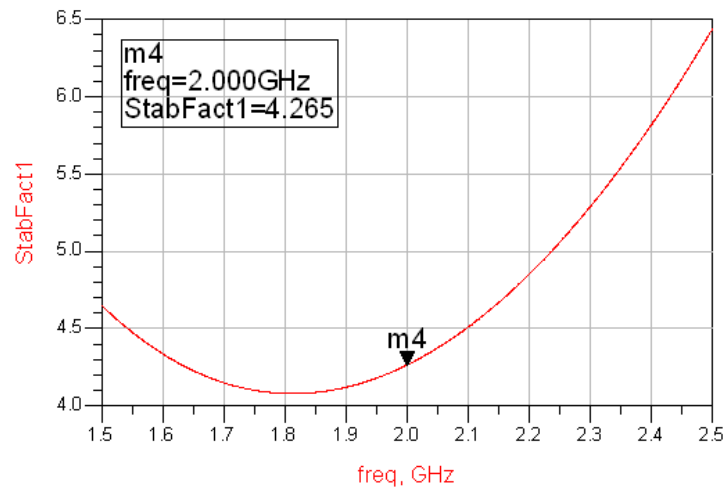


Figure 4. Stability Factor

The S-param simulation shows the LNA gain and the return loss < -10 dB at 2 GHz in Figure 5. This essentially infers that the LNA gain is 19 dB at 2 GHz, which is the frequency the LNA's impedance is matched.

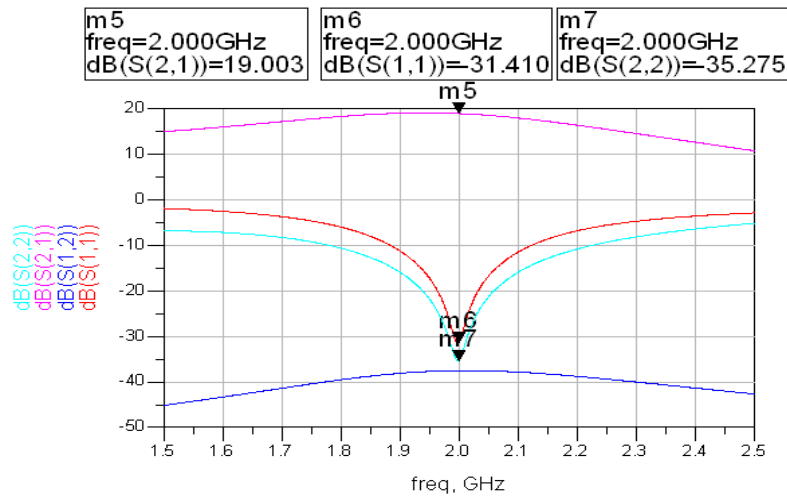


Figure 5. S-Parameter Simulation Results for Gain and Return Loss

Figure 6 shows the Noise Figure simulation results for the developed LNA. The LNA requires a very low noise figure the simulated NF is 1.15 dB.

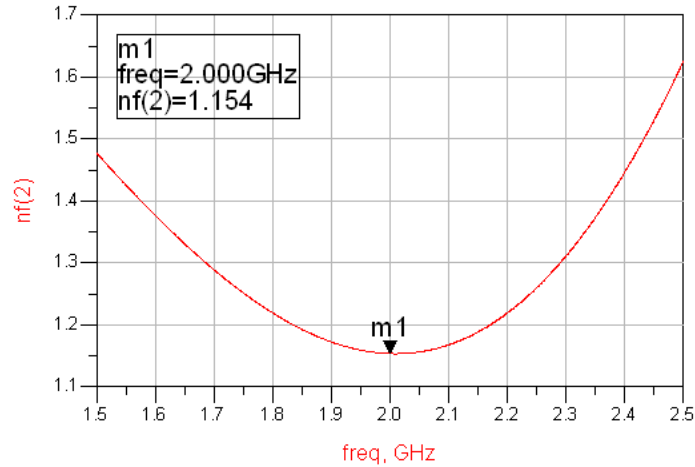


Figure 6. Noise Figure [NF(2)]

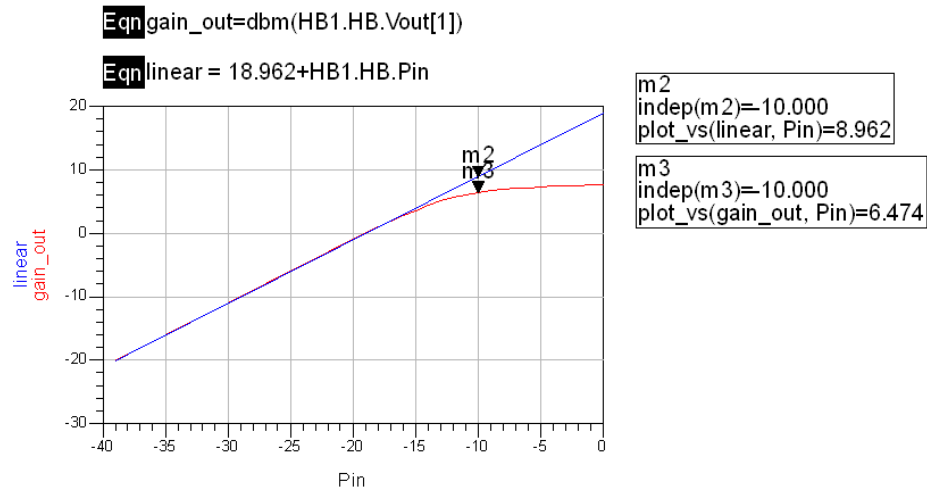


Figure 7. P1dB Compression Point

1dB compression point analysis is carried out to find out the active components linear dynamic range. The output power varies over a range of -9dBm linearly with respect to the input power upto -10dbm. Figure 7 depicts the simulation results of the P1dB compression point.

Low and High Side Output TOI Points, dBm		Low and High Side Input TOI Points, dBm	
15.952	15.971	-3.059	-3.040
Low and High Side Output 5thOI Points, dBm		Low and High Side Input 5thOI Points, dBm	
5.476	5.478	-13.535	-13.533

These become invalid as the amplifier is driven into compression. If the low and high side TOI points do not agree, try increasing the order of each tone and/or the maxorder.

Figure 8: Third Order Intercept Simulation Results

The linearity simulation has been carried out and the TOI is 15.85 dBm.

3.3. Result Analysis

Analysis of these simulation results infer that the circuit requires a supply voltage of 1.2V for center frequency of 2 GHz. Stabfact1 deduces that system is absolutely stable. $S[2,1] = 19.1$ dB gain to meet the design requirements. $S[1,1] = -31.026$ dB, $S[2,2] = -34.799$ dB good input and output matching. Input 1 dB compression point -9 dBm meet the design requirements. $nf(2) < 2$ Description noise figure to meet the requirements; and figure (NFmin) = 1.1 dB, the possibility of further improvement of the system noise figure. The power consumption is only about 3mW, the reason may be due to the use of inductance and capacitance are realized as ideal components, and actual component losses are not considered.

4. Patch Antenna Design

The developed LNA is further interfaced to the square truncated edge-fed right circularly polarized patch antenna. The antenna is developed on Agilent EMpro to facilitate easy export to ADS platform for further co-simulation. The microstrip antenna is one of the most commonly used antennas in applications that require circular polarization. This paper further explicates design of a circularly polarized microstrip antenna that would operate in the 2 GHz range for TDD 2000 system.

4.1 Antenna Design and Simulation

The rectangular patch antenna is the most commonly used microstrip antenna. It is usually operated about the half-wave resonance frequency to obtain nominally real-valued input impedance. The fringing fields act to extend the effective length of the patch, thus the length of the patch is usually less than a half wavelength in the dielectric medium. The design parameters define the operation and the performance of the antenna. The operating frequency determines the size of the patch antenna: $W \approx L = 0.4 \lambda$, while truncation t/W , as well as vertical height of the ground plane, the axial ratio. The ground plane size controls the gain of the antenna while the distance between ground plane and the patch affects the bandwidth. On the other hand, the size of the feed gap influences the impedance matching [5]. The geometry was drawn and the parameters of the antenna optimized through simulations performed in Agilent EMpro. The antenna dimensions are given the Table 1. Figure 9 the model of the patch antenna, the final design parameters.

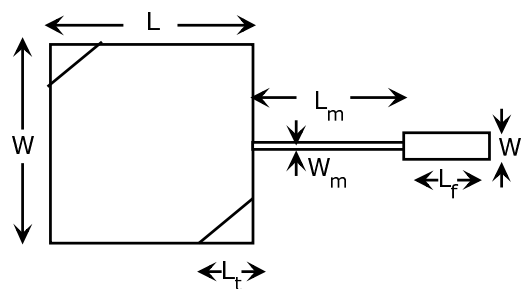


Figure 9. Edge Fed Circularly Polarized Patch Antenna

Subsequent to the antenna designed the $S[1,1]$ or the return loss is analysed using the FDTD engine present in the EMpro simulator. Figure 10 shows the patch antenna developed on EMpro. The simulation results in Figure 11 show that a resonance at 2 GHz is obtained. Further the

radiation patterns are plot in 2D and 3D. The Azimuth gain is around 6.1 dB as shown in Figure 12.

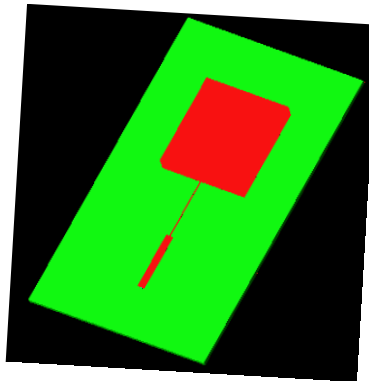


Figure 10: Antenna Design on EMpro

Table 1. Antenna Dimensions

Patch Length (L)	35.65 mm
Patch Width (W)	35.65 mm
Truncated Length (Lt)	2.365 mm
Matching Line Width (Wm)	480.3e-3 mm
Matching Line Length (Lm)	21.84 mm
Feed Line Width (Wf)	2.892 mm
Feed Line Length (Lf)	20.63 mm
Substrate Thickness (H)	1.5 mm
Relative Permittivity (ϵ)	4.35
Loss Tangent ($\tan\delta$)	0.02
Polarization	Right Circular

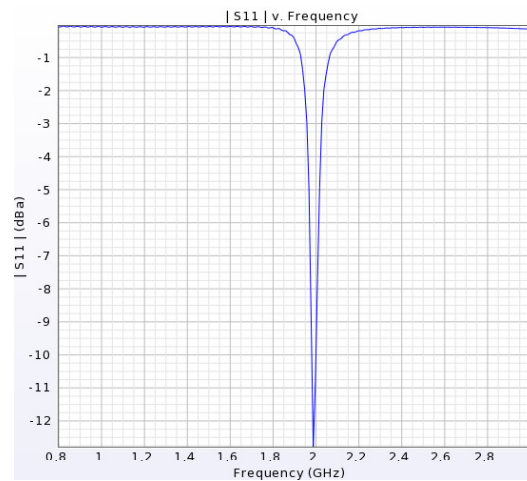


Figure 11. Antenna Return Loss S[1,1]

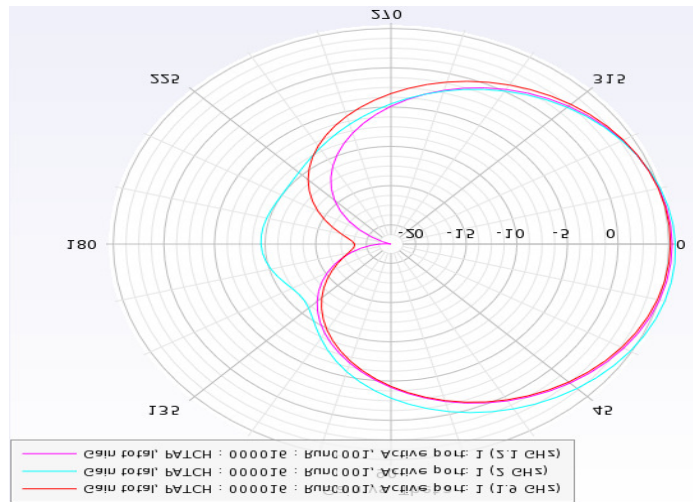


Figure 12: Polar Plot of Azimuth Radiation Pattern

The analysis using the 3D plot shows the total gain > 6.9 dB in Figure 13.

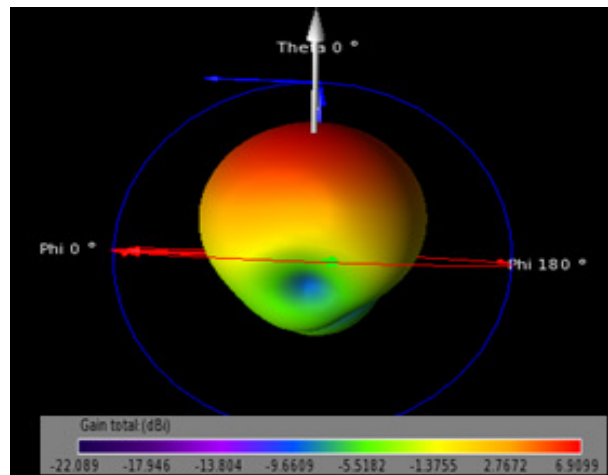


Figure 13. 3D Radiation Pattern of Patch Antenna

5. Cascading Antenna and LNA

The developed cascade LNA and Right Circularly Polarized Patch Antenna are interfaced and co-simulation is performed. The ADS and EMpro simulation platforms are used for co-simulation. Figure 14 shows the antenna and LNA co-simulation as a circuit component in ADS. The HB simulation engine is used for exciting the source.

Figure 15 shows the input and output time domain signals of the developed system. Figure 16 shows the frequency domain response of the input and output signal. The gain of the LNA and P1dB point can be further validated.

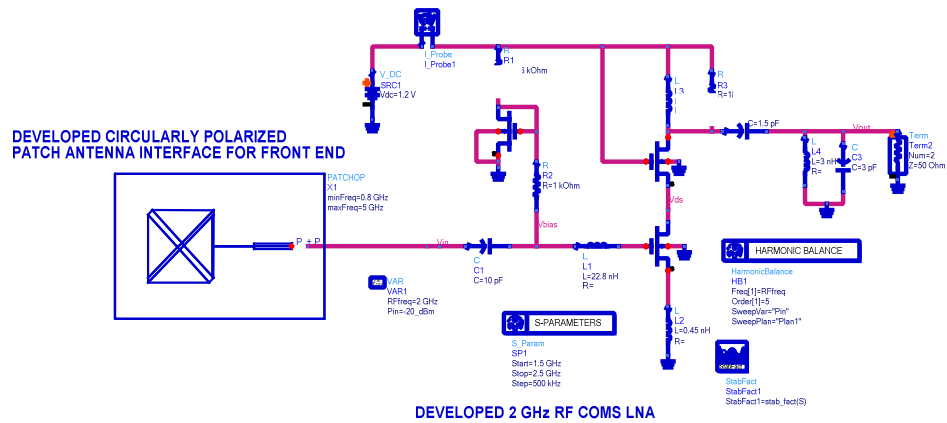


Figure 14. Circularly Polarized Patch Antenna Interfaced with 2 GHz Cascode LNA Co-Simulation

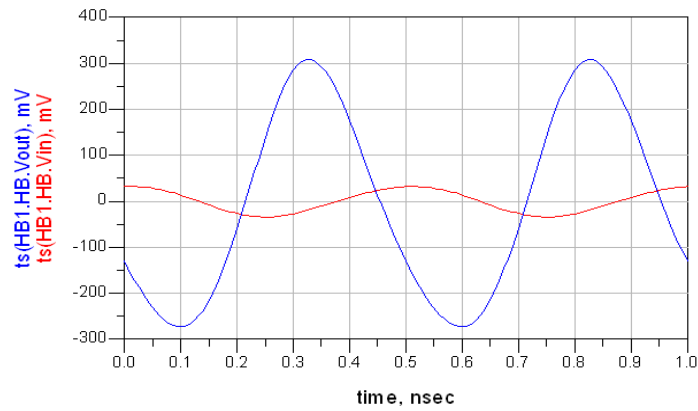


Figure 15: Input and Output Time Domain Signals

m8 freq=2.000GHz dB(HB1.HB.Vin)=-29.666	m9 freq=2.000GHz dB(HB1.HB.Vout)=-10.866
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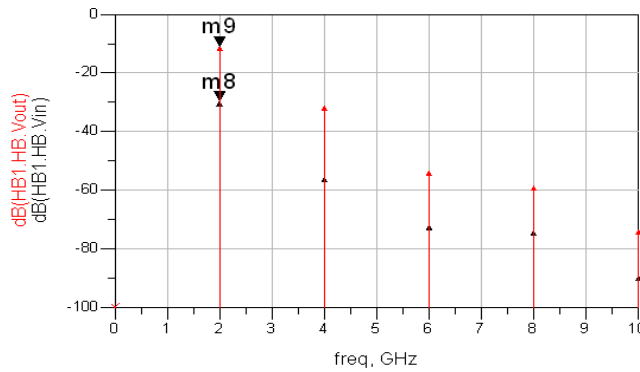


Figure 16: Input and Output Spectrum.

6. CONCLUSIONS

This paper analyzes and design a cascode structure of the low-noise amplifier integrated to a circularly polarized patch antenna which forms the front end for TDD 2000 LTE standard. The low-noise amplifier has lower power consumption and gain provided is adequate for higher gain applications in TDD 2000 standards. A circularly polarized patch antenna developed using EMpro provides high gain for mobile LTE standard. ADS software simulation, optimization, design of LNA performance and the debugging process has been carried out for Antenna interfaced LNA. The use of the ADS software for computer-aided design of LNA and Antenna greatly shorten the development cycle and improve the performance of modular parts.

REFERENCES

- [1] Frank Ellinger (2004) “26-42 GHz SOI CMOS Low Noise Amplifier”, IEEE Journal of Solid-State Circuit, Vol. 39, No. 3, pp522-528.
- [2] Zhangfu Hong, Luo, (2011) “Wireless receiver low noise amplifier design and simulation”, Electronic devices, Vol. 34, No. 1, pp44-48.
- [3] Yongming, (2006) Low Power CMOS low noise amplifier design, Microelectronics, Edn. 5, pp670-678
- [4] Phillip E.Allen, Douglas R. Holberg, (2005) CMOS Circuit Design, Publishing House of Electronic Industry, Edn. 3, pp15-56.
- [5] Marwa Shakeeb, (2010) Circularly Polarized Microstrip Antenna, Master Thesis, Concordia University