HiPDN: A POWER DISTRIBUTION NETWORK FOR EFFICIENT ON-CHIP POWER DELIVERY AND FINE-GRAIN LOW-POWER APPLICATIONS

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ABSTRACT

While the semiconductor roadmap is about to locate in 16nm-FinFET (or Tri-Gate) era, power budget is being entitled major concern to contemporary electronics and future nanometer devices. In this work, a new Power Distribution Network (PDN), referred to as HiPDN, is disclosed for further fine-grain power saving and higher power integrity for supplies in multi-voltage domains. The proposed PDN employs two types of Integrated Voltage Regulators (IVR) with large difference in voltage regulation range. By combining the proposed PDN with the Adaptive Voltage Scaling (AVS) technique, voltage guard-bands can be mitigated to lower the safety margin for voltage variation, i.e., reducing DC set points, thereby effectively decreasing the overhead of power dissipation. In comparison to existing PDNs, theoretical results with a simple equivalent circuit model demonstrate an increase of power saving achieved by HiPDN, thus, allowing longer battery life. Finally, this work provides an on-chip power delivery methodology to improve power efficiency and a simple model to evaluate a PDN and its IVRs.

KEYWORDS

Power distribution network, integrated voltage regulator, power saving, adaptive voltage scaling

1. INTRODUCTION

Over decades, technology scaling which results in significant miniaturization of transistors has brought enormous benefits to the semiconductor industry, such as devices with lower power supply, higher compactness, more powerful performance and etc [4]. However, since 90nm node, transistors have been scaled in an inconsistent track lacking several figures of merit, such as doping concentrations, threshold voltage, and operating speed. So far, Moore's law predicts downsize scaling to 7nm technology node or even more [23]. Under this circumstance, circuit designers are facing various challenges such as tight power budget without degradation in performance, variability in manufacturing or parametric variation, logic failures incurred from different sources, high-energy particles, temperature sense, electro migration and etc [11]. Among these challenges, the energy-efficiency issue has gained special attention from designers.

In literature, various techniques for energy-efficient computing have been developed [2,23,11]. Among them, two well-known power-saving techniques, which are Dynamic Voltage and Frequency Scaling (DVFS) and Power Gating (PG), have been implanted in the latest commercial products [15,20,8,25,10]. In practice, DVFS has been extended into full DVFS, or per core DVFS, for the purpose of fine-grain voltage regulation [27,8,25,10]. The latter PG technique has also been introduced as fine-grain improvement [7,10], where voltage regulation plays a strategic role.

In many cases, the promising capabilities of DVFS and PG have been stemmed by slow off-chip voltage regulators. For example, in DVFS the voltage supply and working frequency are adaptively adjusted which results in minimum power consumption without affecting the performance level. Due to slow off-chip voltage regulators, a considerable amount of energy is wasted while the supply voltage is slowly rising and/or falling correspondingly to frequency transition. The effectiveness of DVFS also significantly relies on the regulator's efficiency and transient response. As a result, the concept of Fully Integrated Voltage Regulator (FIVR) has been introduced and realized in Haswell processors [15], and Integrated Voltage Regulator (IVR) has been implemented in POWER8 processor [8, 25]. IVR- or FIVR-based on-chip Power Distribution Network (PDN) has drawn much attention.

In this paper, a novel PDN is presented to support fine-grain improvement in power-efficiency. Compared with existing PDNs, the proposed PDN is able to mitigate power dissipations associated with power delivery from source to load. To be precise, when being combined with Adaptive Voltage Scaling (AVS) technique [5], this new PDN enables the reduction of voltage safety margin by guard-banding approach. Voltage safety margin for both minimum voltage and voltage variation is decreased, whereby power saving can be obtained by reducing power consumption of voltage converters.

The rest of this paper is organized as follows: background of PDNs and related works are first reviewed in Section 2. Section 3 presents the proposed PDN and its properties. From this new PDN, power transmission losses, power saving obtained when combined with AVS, and total power consumption are estimated in Section 4. Finally, conclusions are given.

2. RELATED WORK

Since Integrated Circuits (IC) were introduced into commercial products, the PDN illustrated in Fig. 1 has been employed for a long while. The power delivery mechanism in Fig. 1 is straightforward, with a single Voltage Regulator (VR) located on the motherboard [22].

After the very first phase of PDN, in [29], the second phase of power delivery network has been presented, with migration from VR into IVR, as shown in Fig. 2. By utilizing IVR, instead of off-chip VR, several advantages can be obtained, such as, high power integrity, power saving with per-core voltage control, reduced PCB area, nanosecond voltage scaling speed, mitigation on IR loss by power delivery at high voltage and low current, and etc [21, 30-32].

Recently, a more dedicated PDN has been developed in [16, 26], as shown in Fig. 3. In this PDN, two stages of IVRs are utilized for on-chip power supply while an off-chip VR, which is located on the motherboard, provides the input power for IVR-1, as in Fig. 3. IVR-1 down converts the

output voltage of VR and provides power for IVR-2, which in turn regulates its output to support a load, for instance, a CPU core or an SoC. In the routing configuration of Fig. 3, a single IVR-1 is used while multiple IVRs-2 are disposed to support different voltage domains. Based on this PDN, an extension work which couples the PG technique to provide reduction of silicon area on power delivery network is introduced in [9].

3. HIPDN: THE POWER DISTRIBUTION NETWORK

In Fig. 4, the proposed PDN, referred to as HiPDN, is demonstrated. In contrast with the PDN in Fig. 3, multiple IVRs-1 are implemented, instead of a single IVR-1, as shown in Fig. 4. Moreover, regulated power is supplied to the load through three converter stages: VR to IVR-1

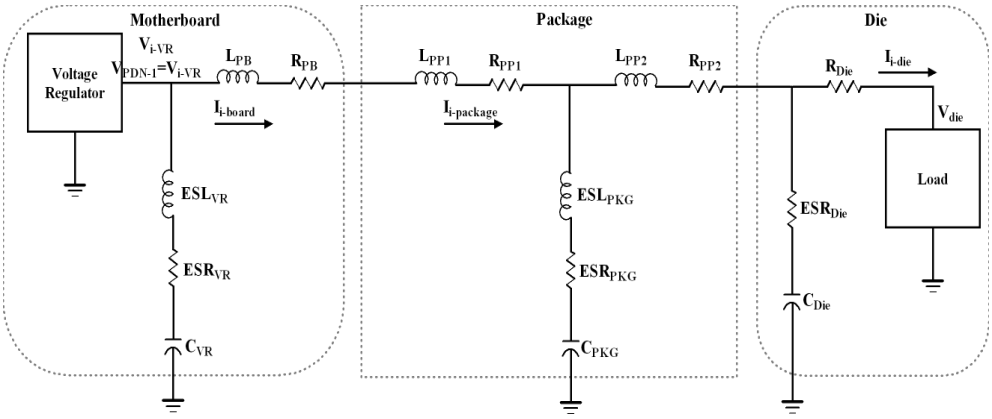

Figure 1.The very first phase of power delivery network, from VRM to IC package.

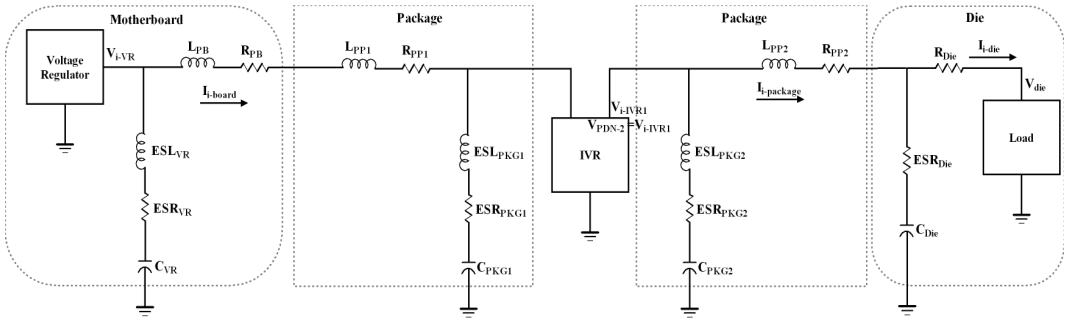

Figure 2. The second phase of power delivery network, from VRM to IVR, then to IC package.

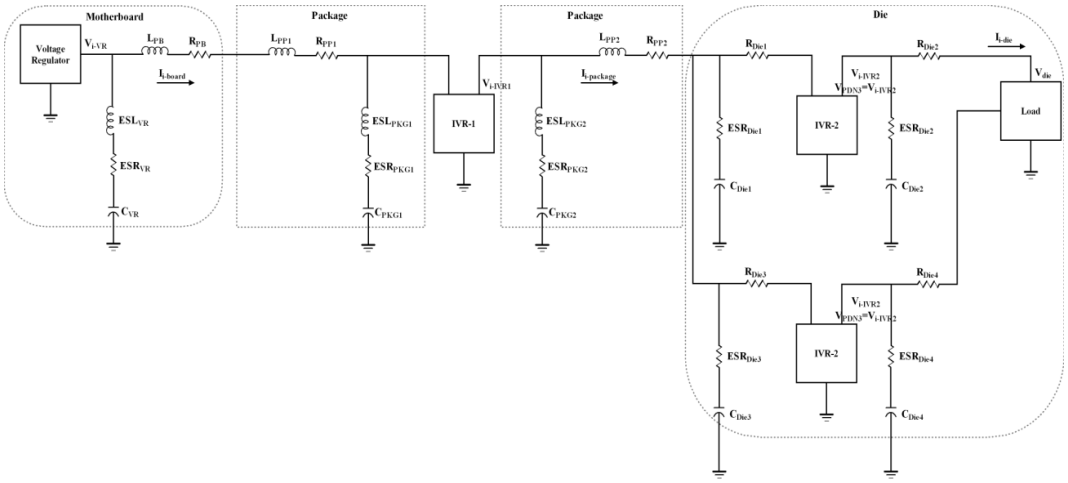

Figure 3. The third phase of power delivery network, from VRM to IVR-1, and conversion from IVR-1 to IVRs-2, then to IC package.

to IVR-2 to load, or two converter stages, VR to IVR-1 to load if it is needed, as shown by the dashed lines and shadowed box in Fig. 4. To explain this voltage regulation mechanism, properties and characteristics of IVRs-1 and IVRs-2 are detailed in Section 3.2.

As a preview of the HiPDN, its contributions can be summarized as following:

- ***Expandability***: Different power conversion stages are designed for the purpose of mitigation on power transmission losses and reduction of DC set point.

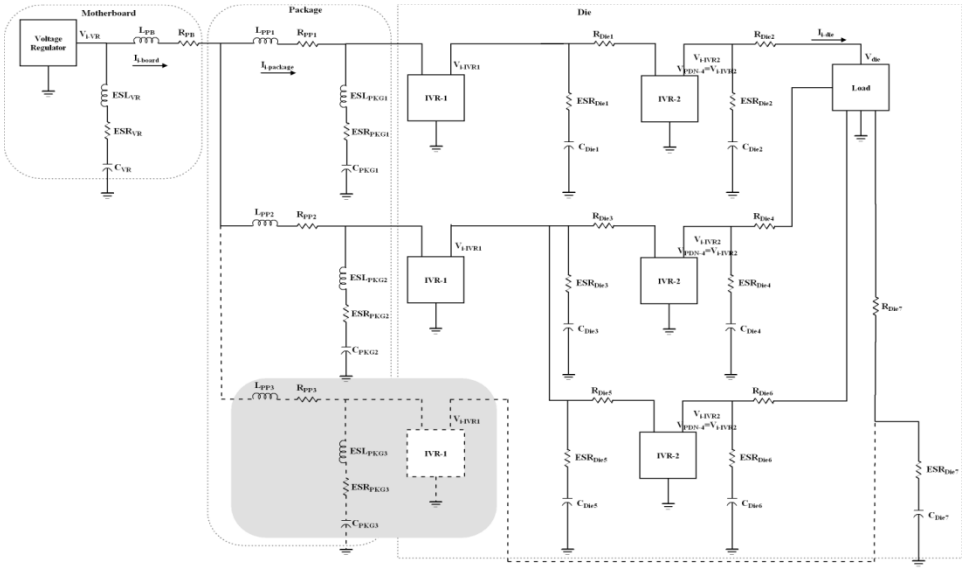

Figure 4. The proposed PDN, HiPDN, for on-chip SoC power supply.

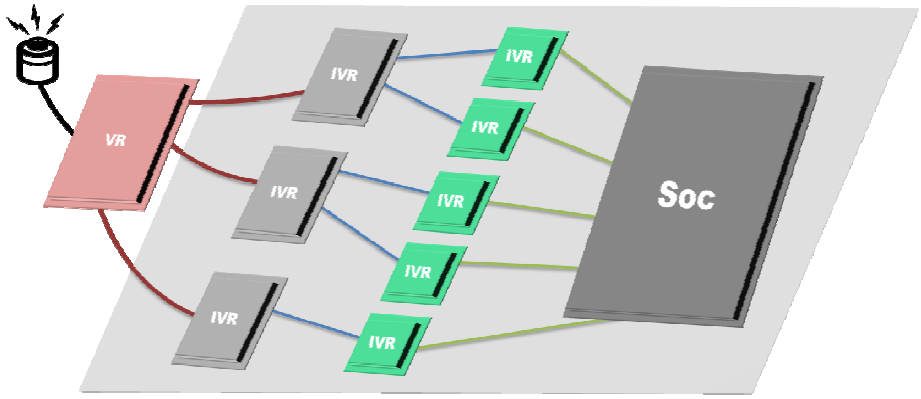

Figure 5. The proposed PDN, HiPDN, with multiple IVRs-1 coupled to VR and conversion from IVRs-1 to IVRs-2 for different voltage domains.

- ***Heterogeneity***: IVRs implemented in this PDN perform large range of voltage regulation and narrow range of voltage regulation in different stages to optimize the efficiency of individual IVRs, per se, and the efficiency of the overall system as well.

- ***Fine-adjustment***: For the forthcoming nanometer devices, high power integrity and high resolution in voltage adjustment not only are a must for circuit's power supply but also enable fine-grain low-power techniques.

- ***Synergy***: In combination with guard-band approach of AVS technique, further power saving can be realized through reduction of voltage safety margin for both minimum voltage set up and voltage variation.

3.1. Expandability: power delivery system

The first main contribution of the HiPDN is the utilization of multiple IVRs-1, instead of a single IVR-1. In practice, multiple-domain DVFS with multiple output levels is required to deliver a wide range of voltage supply for on-line and/or off-line components in a modern System-on-Chip (SoC) architecture. An SoC deploys a considerable amount of computing blocks or subsystems, which can be digital signal processing units, logic computing blocks, RF components, mixed-signal process, analog devices, and etc [7,8,25]. For instance, in the SoC of a modern cell phone, RF transceiver, communication process, memory, application processor, connectivity, camera, display, user interface and audio are powered by Power Management Integrated Circuits (PMIC) [13]. Consequently, a wide range of power level, supply voltage, and working frequency are required for those subsystems.

To regulate and finely adjust multiple voltage supplies over a wide range, multiple IVRs-1 are implemented so that power supply can be provided in an efficient manner, which is discussed in the followings.

3.2. Heterogeneity: designs of IVRs

In this section, the designs of IVR-1 and IVR-2 are explained in details. There are mainly three types of regulators. Linear regulators provide the best integration compactness and transient response, but they compromise efficiency at low output voltage [19]. Similarly, switched-capacitor regulators are able to offer high integration, but they also suffer from voltage-dependent efficiency characteristic. However, several on-chip switched-capacitor regulators have been reported to reach efficiency as high as 90% thanks to the self-regulation capability with stacked voltage domain technique [2,24]. On the contrary, inductive switching regulators achieve high efficiency over a wide range of output voltage levels. Although inductive switching regulators are difficult to fully integrate on-chip due to bulky inductors, they are capable of delivering good transient response with a high level of efficiency [19, 15].

In this work, inductive switching regulator and low-dropout (LDO) regulator have been implemented for IVR-1 and IVR-2, respectively. Since we aim at high efficiency over a wide range of output voltage levels, a buck converter is the choice for IVR-1. For IVR-2, because an LDO achieves high efficiency only if the voltage drop is low while the current efficiency is fixed [3, 14, 18], the difference between input voltage and output voltage of IVR-2 is locked in short range, for instance, $500mV$. In short, multiple IVRs-1 are implemented as the first voltage conversion stage, and the second stage of voltage regulation is carried out by IVRs-2 over a narrow range of voltage drop.

3.3. Fine-adjustment: fine-grain low-power applications

Since the 70's, technology scaling has led to transistor miniaturization and reduced the supply voltage toward an incredible low range [4]. Besides, the turn-on voltage can be further reduced via emergent techniques at fundamental physics level, for instance, the transistors beyond silicon [2, 23, 12]. Currently, foundries still stick to the schedule for the coming tape-out or mass production based on Si FET, for example, TSMC has introduced the FinFET process at 16nm node [1], where supply voltage and threshold voltage are certainly going down.

In other words, the headroom for voltage regulation has been migrated from volts level to lower than a hundred millivolts, so that fine-grain based voltage regulation is achieved [27]. Meanwhile, variations including supply voltage fluctuation have caused reliability concern to modern processes [17, 6]. Therefore, high resolution in voltage step and high Power Integrity (PI) have become important characteristics of power supply. In literature, several LDOs have been reported with featured high resolution in voltage step, as low as $3mV$ in [14].

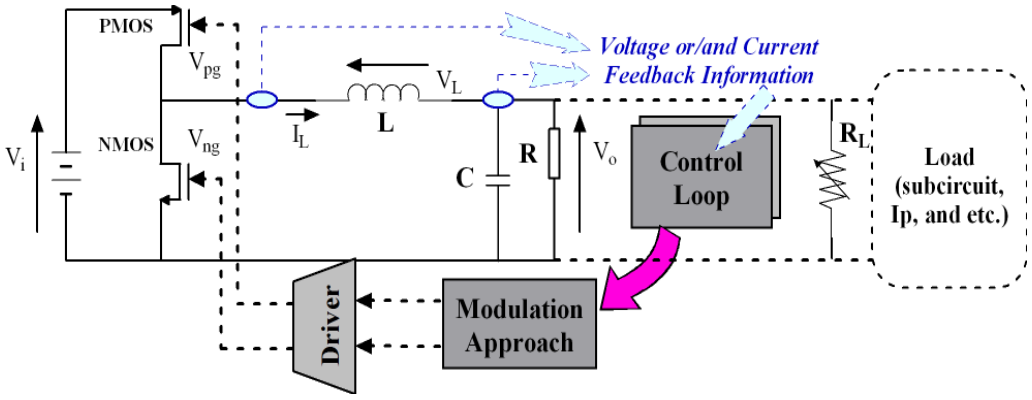

Figure 6. The structure of a buck converter with additional filtering block.

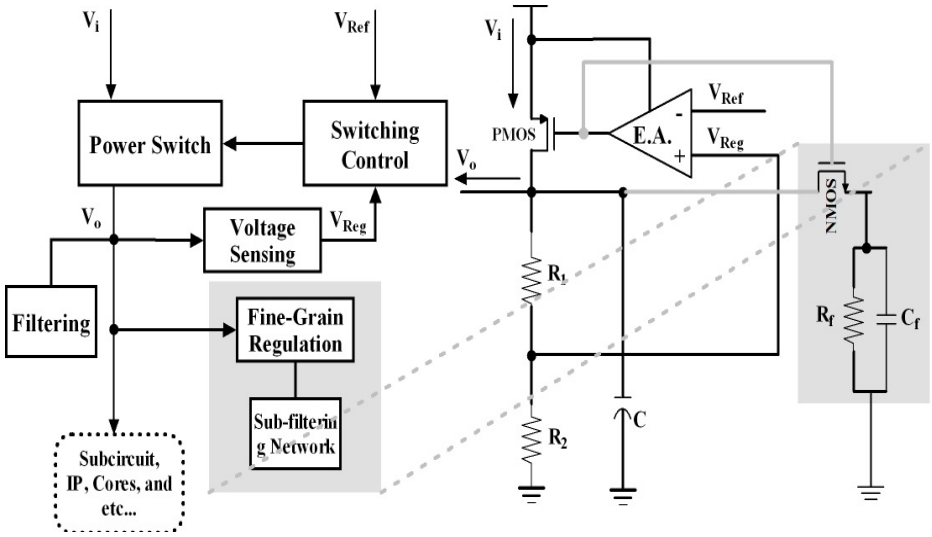

Figure 7. The structure of an LDO with additional fine-grain regulation.

For high PI, in this paper, two noise rejection mechanisms are presented for buck converter and LDO, respectively. In Fig. 6, an error amplifier and a power MOSFET are employed as an extra filtering block for ripple rejection and spike suppression. This mechanism relies on the filtering virtue of LDO, of which similar work has been introduced in [18]. For noise rejection in LDOs, an additional fine-grain regulation line with sub-filtering network is clamped at the load. Beside noise rejection, the fine-grain regulation network also delivers fast transient response.

As a conclusion, since the load supply is provided by LDOs, the LDOs must both reject noise at the input while generating minimal noise at the output and the load. Both buck converter stage and LDO stage are needed to enhance the ability of noise rejection.

3.4. Synergy: combination with AVS

In this section, another major contribution of the HiPDN is presented. Designers may have ignored the implication of PDN to the AVS. In this work, we introduce the connections between the PDN and the AVS so that the power consumption can be mitigated without involving any other power-reduction technique.

In Fig. 8, voltage safety margin is depicted by guard-banding approach. The safety margin is divided into five shares that allow for, process variation, temperature fluctuation, aging issue, voltage variation, and minimum voltage [28]. In fact, DC effect such as IR drop and AC effect such as transient drop by *Idi/dt* raise DC set point. However, increasing DC set point introduces

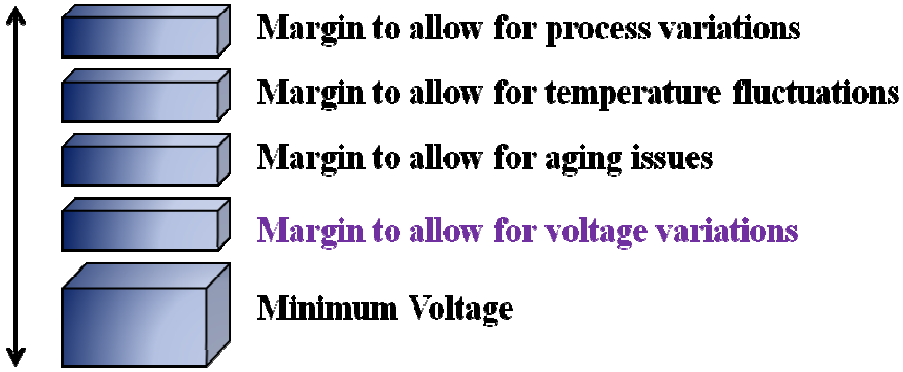

Figure 8. By guard-banding approach, voltage safety margin takes into account process variations, temperature fluctuations, aging issues, and voltage variations.

more power dissipation. Furthermore, the margin for voltage variation raises while bad load condition is met.

The proposed HiPDN provides better resilience to AC effect, see the ***Fine-adjustment*** in Section 3.3 and also decreases the DC set point via the ***Heterogeneity*** introduced in Section 3.2.

4. POWER SAVING ACHIEVED BY HIPDN

In this section, estimations of power saving achieved by HiPDN, without applying any other techniques for energy-efficiency boost, are disclosed. The major reductions on power consumption for power delivery systems are in twofold, mitigation on transmission losses over delivery and reductions on power consumption of regulators via shrinking voltage safety margin.

4.1. Simplified model for transmission losses

From Fig. 1, Fig. 2, Fig. 3, and Fig. 5, the transmission losses for PDN-1, PDN-2, PDN-3, and PDN-4, as the corresponding PDN, can be derived, respectively. For the sake of simplicity, ESRs, ESLs, parasitic resistances, and capacitance have been simplified into three resistive variables,

R_{board}, $R_{package}$, and R_{die}, which represent the equivalent resistance for connects of VR on motherboard, the equivalent resistance for connects of IVRs in package, and the equivalent resistance for connects of ICs or IVRs on die, respectively. Please note that R_{board}, $R_{package}$, and R_{die} represent DC resistor in paths and also AC resistance incurred by parasitic effects, such as the inductance of package leads. Therefore, power consumption for transmission over power delivery P_{tr} can be expressed as,

$$P_{tr} = \sum_{i=1}^{N}(I_{i-board}^2(R_{board} + jR_{package}) + I_{i-package}^2(R_{package} + kR_{die}) + I_{i-die}^2 R_{die}) \quad (1)$$

where $I_{i\text{-}board}$, $I_{i\text{-}package}$, and $I_{i\text{-}die}$ represents the resultant current from power regulators flows through related board, package, and die, respectively, for each load supply, $\boldsymbol{j}$ and $\boldsymbol{k}$ are variable from the binary set (0, 1). Since different topologies are involved from Fig. 1 to Fig. 4, configurations by $\boldsymbol{j}$ and $\boldsymbol{k}$ enable different connects for packaging and different connections for die. $\boldsymbol{N}$ represents the number of load supply, for instance, $\boldsymbol{N}$ equals to 2 in the case of Fig. 3. Moreover, for resultant currents from different power regulators, each of them depends on the transmission voltage across different ends while total power supply to load P_{ps} is constant, as described as,

$$P_{ps} = \sum_{i=1}^{N} I_{i-die} V_{i-die} \quad (2)$$

where $I_{i\text{-}die}$ and $V_{i\text{-}die}$ represent the supply current to load and the supply voltage to load, respectively, which are defined by specifications.

4.2. Simplified model for power consumption of regulators

Besides transmission losses, power consumptions by regulators are also regarded as significant proportions to total power consumption. In order to estimate the power consumption of regulators P_{reg}, a simple model is introduced, here, based on resultant voltage, resultant current and efficiency of regulator, as follows,

$$P_{reg} = \sum_{i=1}^{N}(I_{i-board} V_{i-VR}(\frac{1}{E_0} - 1) + I_{i-package} V_{i-IVR1}(\frac{1}{E_1} - 1) + I_{i-die} V_{i-IVR2}(\frac{1}{E_2} - 1)) \quad (3)$$

where $V_{i\text{-}VR}$, $V_{i\text{-}IVR1}$, and $V_{i\text{-}IVR2}$ represent the output voltage from off chip voltage regulator, the output voltage from IVR-1, and the output voltage IVR-2, respectively. Moreover, $\boldsymbol{E_0}$, $\boldsymbol{E_1}$ and $\boldsymbol{E_2}$ define the efficiency of off-chip regulator, the efficiency of IVR-1, and the efficiency of IVR-2, respectively. While power supply to load is constant according to specification, as shown in (2), load current and voltage drop for each end are differed for different power delivery systems. Nevertheless, resultant voltages from different regulators are all composed of three proportions; minimum voltage, transient voltage drop, namely transient response incurred by load change, e.g., IR drop and *di/dt-drop*s caused by parasitics resistances and inductance. Thus, the DC set points for different regulator can be expressed as,

$$V_{PDN-1} = V_{i-die} + td_1 + I_{i-board}(R_{board} + R_{package} + R_{die}) \quad (4)$$

$$V_{PDN-2} = V_{i-die} + td_2 + I_{i-package}(R_{package} + R_{die}) \quad (5)$$

$$V_{PDN-3} = V_{i-die} + td_3 + I_{i-die} R_{die} \quad (6)$$

$$V_{PDN-4} = V_{i-die} + td_4 + I_{i-die}R_{die} \quad (7)$$

where V_{PDN-1}, V_{PDN-2}, V_{PDN-3}, and V_{PDN-4} are DC set point for PDN-1, PDN-2, PDN-3, and PDN-4, respectively. Also, td_1, td_2, td_3, and td_4 are transient voltage drop for PDN-1, PDN-2, PDN-3, and PDN-4, respectively. From (4)-(7), DC set point depends on the structure of delivery system, as explained in Section 3.2. Furthermore, resistive voltage drops are proportional to equivalent DC resistance and as well AC resistance. In fact, supply grids within shorter distance to loads introduce smaller voltage drops caused by parasitic resistance.

4.3. Estimation on total power saving

With (1) and (3), the power consumption for power delivery system P_{total} can be concluded as the sum of transmission losses and power dissipations of regulators as written as follows,

$$P_{total} = P_{tr} + P_{reg} \quad (8)$$

In this work, the simulated power supply scenarios are four power supplies, *Vdds*, as $0.9V$, $1.2V$, $1.5V$, and $1.8V$, with identical load current of $10A$ for each. In addition, voltages resulted from different regulators should meet the minimum level requirement as power supply to load is constant, see (2). Hence, resultant voltages of regulators in different PDNs are deductable.

First, in Fig. 9, total power losses of PDN-2 and PDN-4, normalized to PDN-1, are compared over a range of R_1 from 0.001Ω to 0.2Ω, and from 0.001Ω to 0.1Ω to for R_2, while $R_3 = 0.001\Omega$. In addition, td_1, td_2, and td_4 are $0.32V$, $0.08V$, and $0.003V$, respectively. Also, E_0 and E_1 are both fixed at 95% and current efficiency as 100% for IVR-2. As illustrated, PDN-2 offers more than 30% reduction of total power loss when R_1 addresses significant large resistance and R_2 are, on the contrary, in small resistance. However, if R_1 is fixed as high as 0.1Ω, PDN-2 is not producing gain in power saving with comparison to PDN-1, unless R_2 drops as low as

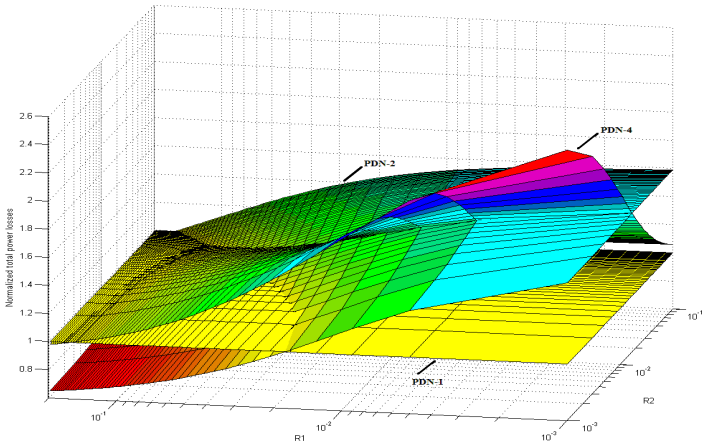

Figure 9. Normalized total power losses of three PDNs versus R_1 and R_2 when td_1, td_2, and td_4 are $0.32V$, $0.08V$, and $0.003V$, respectively. Additionally, E_0 and E_1 are both fixed at 95%, and current efficiency as 100% for IVR-2, with $R_3 = 0.001\Omega$.

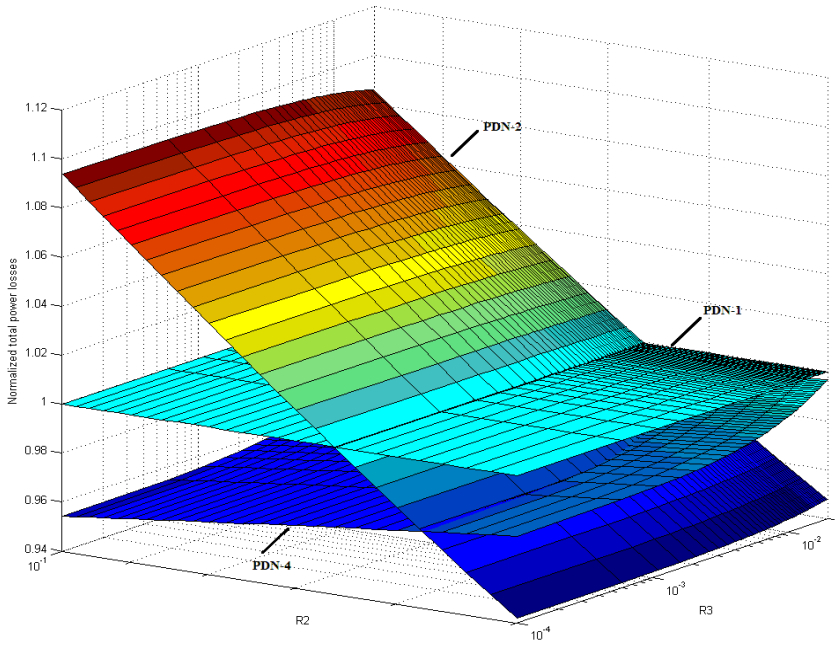

Figure 10. Normalized total power losses of three PDNs versus R_2 and R_3 when td_1, td_2, and td_4 are $0.32V$, $0.08V$, and $0.003V$, respectively. Additionally, E_0 and E_1 are both fixed at 95%, and current efficiency as 100% for IVR-2, with $R_1 = 0.1\Omega$.

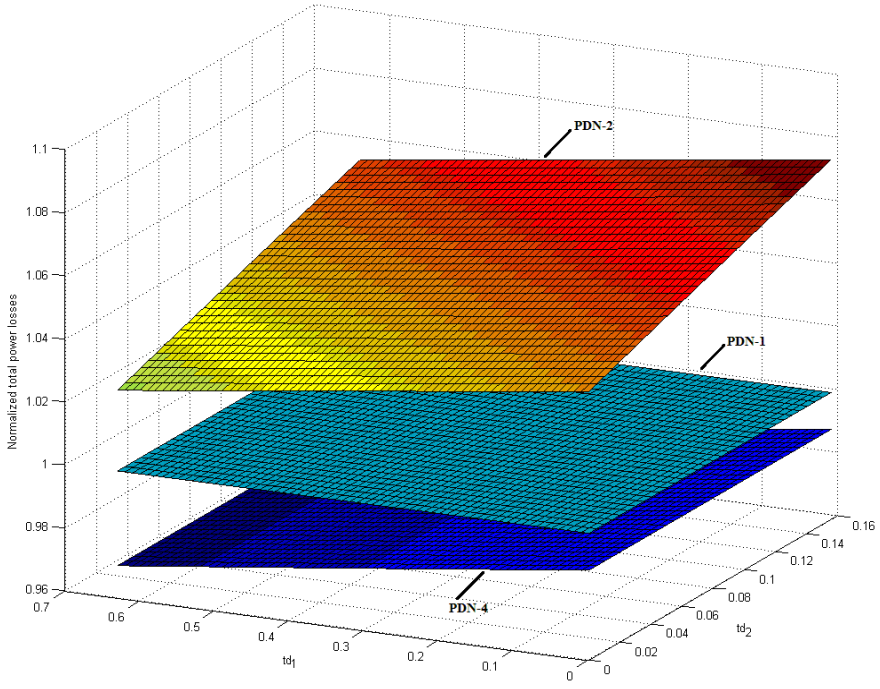

Figure 11. Normalized total power losses of three PDNs versus td_1 and td_2 when R_1, R_2, and R_3 are 0.1Ω, 0.05Ω, and 0.01Ω, respectively. Additionally, E_0 and E_1 are both fixed at 95%, and current efficiency as 100% for IVR-2, with $td_4 = 0.003V$.

close to 0.65Ω, as shown in Fig. 10. In contrast, PDN-4 is able to generate reduction on power losses in the sweeping range for R_2 from 0.05Ω to 0.1Ω, while R_3 is swept from 0.0001Ω to 0.02Ω. Therefore, PDN-2 enables reduction on power consumption while equivalent resistance through package R_2 is small enough, i.e., the ratio of resistance through package R_2 to resistance through motherboard R_1 is sufficiently small. Meanwhile, PDN-4 achieves lower power losses even in the case of large resistance R_2. One should note that PDN-3 is not discussed in the work because its total power consumption is not good in comparison to the remaining three PDNs.

Second, by sweeping the transient voltage drop for PDN-1, td_1, and the transient voltage drop for PDN-2, td_2, normalized power losses of PDN-2 and PDN-4 to PND-1 are demonstrated in Fig. 11, with constant td_4 of 0.003V. It can be observed that PDN-4 obtains gain in power savings while td_1 is swept from 0.001V to 0.64V and td_2 is swept from 0.001V to 0.16V, but for PDN-2, its power consumption increases instead. While Fig. 11 is generated with R_1, R_2, and R_3 are fixed at, 0.1Ω, 0.05Ω, and 0.01Ω, respectively, Fig. 12 is obtained with R_1, R_2, and R_3 are 0.1Ω, 0.025Ω, and 0.005Ω, respectively. From Fig. 11 and Fig. 12, it can be seen that PDN-2 delivers large power savings only if R_2 is regarded as a small proportion to R_1. In contrast, PDN-4 enables power reduction even in a power delivery system with large resistance through motherboard as well as for resistance through package and large resistance through die.

Third, Fig. 13 illustrates the effect of both off-chip regulator's efficiency and IVR-1's efficiency on the power saving performances of PDN-4 and PDN-2 relative to that of PDN-1, by sweeping E_0 and E_1, while R_1, R_2, and R_3 are set as 0.1Ω, 0.05Ω, and 0.01Ω, respectively. It can be seen that PDN-4 achieves power saving without placing stricter requirements on the design of the voltage regulators as compared to PDN-2.

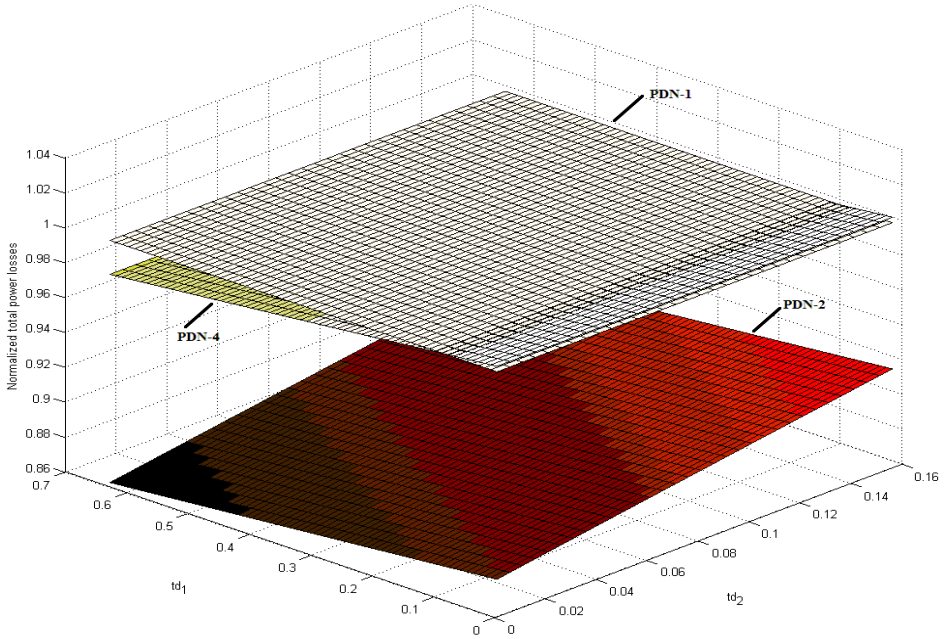

Figure 12. Normalized total power losses of three PDNs versus td_1 and td_2 when R_1, R_2, and R_3 are 0.1Ω, 0.025Ω, and 0.005Ω, respectively. Additionally, E_0 and E_1 are both fixed at 95%, and current efficiency as 100% for IVR-2, with td_4 = 0.003V.

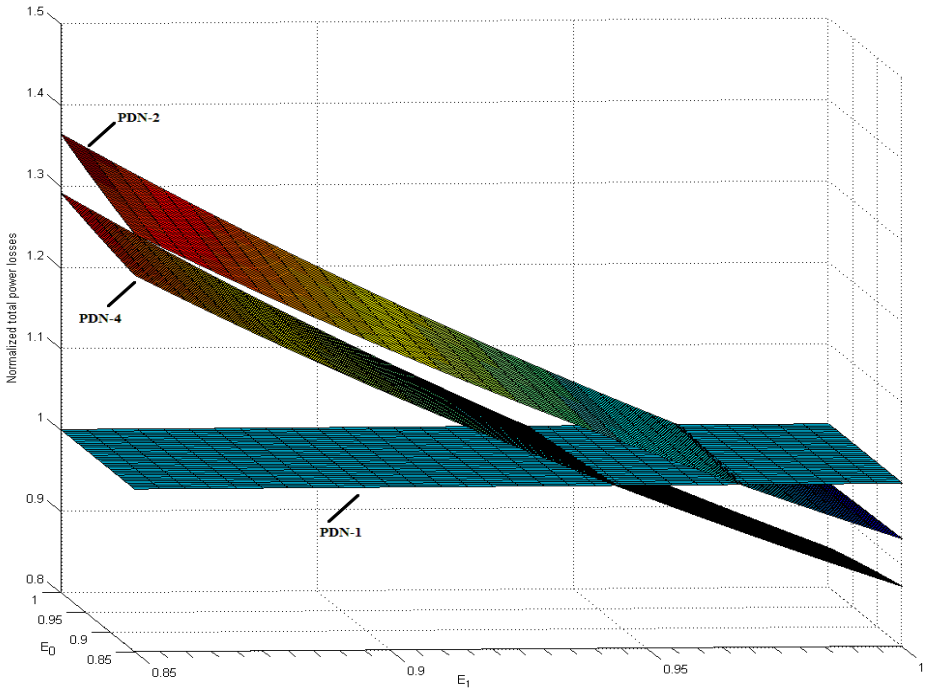

Figure 13. Normalized total power losses of three PDNs versus E_0 and E_1 when R_1, R_2, and R_3 are 0.1Ω, 0.05Ω, and 0.01Ω, respectively. Additionally, current efficiency for IVR-2 is fixed at 100%, with $td_1 = 0.32V$, $td_2 = 0.08V$, and $td_4 = 0.003V$.

To sum up, the following conclusions can be drawn,

- With comparison to PDN-1 and PDN-4, PDN-2 is able to deliver large reduction in power consumption only if small resistance (including DC and AC effects of parasitics) is assumed in the power delivery system, especially, the resistance through package.

- In contrast, the power saving advantage of PDN-4 is relatively insensitive to parasitic in the power delivery system. Power saving can still be achieved by adopting PDN-4 in a system with large resistances R_1, R_2, and R_3.

- For both PDN-2 and PDN-4, voltage regulators are required to have high efficiency to enable power reduction. Nevertheless, in comparison with PDN-2, PDN-4 requires lower efficiencies for VR and IVR-1 to achieve the same amount of power reduction.

6. CONCLUSIONS

As energy-efficiency becomes a major concern, circuit designers have spent much effort to improve the performance of power distribution network (PDN) so as to lower power budget. By employing two types of Integrated Voltage Regulators (IVR) with large difference in voltage regulation range, the proposed PDN, referred to as ***HiPDN***, enables power saving and higher power integrity for supplies in multi-voltage domains. First, the HiPDN achieves the reduction of

transmission losses associated with power delivery. Second, when being combined with the voltage guard-banding approach from the Adaptive Voltage Scaling (AVS) technique, the proposed PDN reduces voltage safety margin for minimum supply voltage and as well voltage variation, and thus additional power saving can be achieved. In comparison with existing PDNs, theoretical results based on a simple equivalent circuit model demonstrate an increase of power efficiency achieved by HiPDN via reduction of transmission losses and lower dissipations by voltage regulators themselves. As a consequence, extending battery life can be achieved when HiPDN is applied. Additionally, this theoretical analysis model is suitable to guide the design of PDNs and IVRs.

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