ANALOG TO DIGITALCONVERTOR FOR BLOOD-GLUCOSE MONITORING

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ABSTRACT

This paper presents the design of a low-power CMOS current-frequency (I–F) Analog–Digital Converter. The ADC is designed for implantable blood-glucose monitoring. This current frequency ADC uses nA-range of input currents to set and compare voltage oscillations against a self-produced reference to resolve 0–32nA with an accuracy of 5-bits at a 225MHz sampling rate. The comparator used is a dynamic latch comparator and the output is fetched from a 5-bit counter. This is designed in 180nm CMOS technology with a supply of 1.8V, it operating voltage taken here is 0.0- 1.8V with power consumption of 12.3nW using Cadence tools.

KEYWORDS

Current-frequency ADC; Low power; Dynamic Latch comparator

1.INTRODUCTION

Blood glucose meters measure the amount or the concentration of glucose in blood (glycaemia) of diabetics patient allowing for the administration of the proper dose of insulin to maintain balance. Particularly important in the care of diabetes mellitus. Blood glucose meters are small computerized machines that "read" your blood glucose, then applying the blood to a chemically active disposable 'test-strip'. Different manufacturers use different technologies, but most of them, measure an electrical characteristic, and further use this to determine the glucose level in the blood. There are many meters to choose from.

Monitoring and correcting the sugar level in the body accurately requires a sensitivity of 2 mg/dL across a range of 20 to 600 mg/dL, or about eight bits of accuracy. However, 5-bits accommodate an accuracy of 10 mg/dL across dangerously low and high extremes, from 20 to 340 mg/dL, offering considerable value to the patient.

The ADC must resolve the current that a miniaturized ampere-metric glucose sensor generates, which is typically in the range of 1 μA to 1 *n*A which in this case can reach up to 31*n*A with 5-bits of resolution. Similarly, because miniaturized kinetic harvesters can generate less than 10μW, the design aims to dissipate around 1μW. As alluded earlier, the time constant associated with glucose variations in the body is on the order of minutes, so over-sampling the system at around 100 Hz is sufficient.

2. Organization of the paper

This paper presents a current–frequency (I–F) analog to digital convertor working at 180 nm CMOS ADC that is able to resolve nA's to within five bits of accuracy while drawing 1.1nA from a 1.8-V supply. In this design a comparator [2] is used to compare the input value with the reference voltage, a 5-bit counter [3] to get 5-bit output which further fetch to controller to find the value of glucose in the blood by 5 bit latch [4]. The input range that the proposed ADC receives corresponds to what ampere-metric sensors produce and the power level it requires to operate is within the range that energy-harvested systems can supply [1].

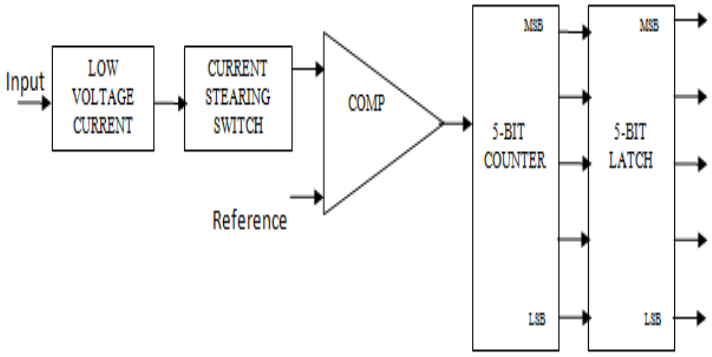

Figure 1 Block Diagram of Current-Frequency ADC

The block diagram of I-F ADC is shown in Figure 1 in which, the input signal given to input stage (contains low voltage current mirror and current steering switch)to drive the current to comparator, then comparator will compare this value with the reference signal. Now we get a data which we fetch to counter for getting the desired bits output.

3. Circuit Design

Frequency-based ADCs generally match the low-power and low-speed requirements that harvester-powered ampere-metric glucose monitors impose. More particularly, because glucose sensors ultimately generate a current, directing input current into the capacitor of a ramp-based oscillator converts current into frequency directly, which means current–frequency ADCs of this sort need not include additional power-consuming stages to condition the input. What is more, the integrating capacitor inherent in these ADCs filters unwanted noise.

3.1 Schematic of I-F ADC

Current-frequency ADC is basically a voltage-to-frequency converter (VFC) and is an oscillator whose frequency is linearly proportional to a control voltage. In this schematic we are feeding input to the current mirrors, to drive the input to the comparator. As shown in Figure 2, cascode-mirrors NM2–NM10 and PM0–PM4 receive and fold input current i_1 or I_R so switches PM5 and PM6 can stear it into or away from integrating capacitor C_1(1pF).

Comparator senses C1 voltage VC to determine the connectivity of NM0 and PM5. PM6 And NM1 keep the mirrors conducting to the supply and ground when their corresponding switches NM0 and PM5 are off, so the mirrors do not suffer from start-up delays, which would otherwise extend the delay across the loop (i.e., increase td and distort VC's ramp.

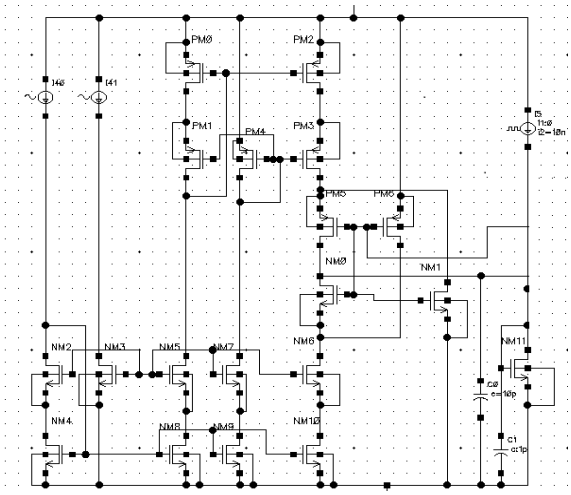

Figure 2 Schematic of Current mirror and current steering circuit

Now as we give an analog signal at the input, it first goes through the current mirror and current steering circuit, then this signal is compared with the reference signal at frequency of 225 MHz and a voltage of 1.8V.

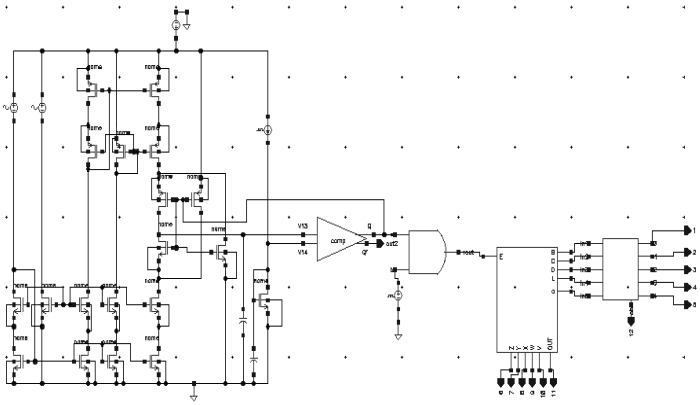

Figure 3 Schematic of Current-Frequency ADC

The output of comparator is given to counter which separate this digital signal into 5 different samples, which is latched through which we get output of 5-bit resolution.

This resolution is calculated by the formula

$$resolution = log_2(\frac{VF_S}{\delta V}) \qquad (1)$$

Where VF_S is full-scale output voltage range
δV is full-scale input voltage range

3.1.Dynamic Latch Comparator

The comparator comprised of three blocks, an input stage (current mirror and a current steering circuit), a flip-flop block and SR latch block. This architecture uses two non-overlapping clocks

(φ1 and φ2) shown in Figure 4, which operates in two modes, reset mode during φ2 and regeneration mode during φ1.

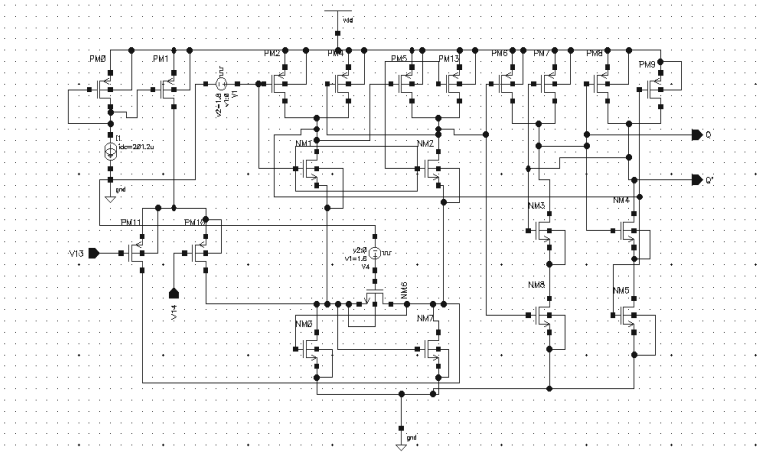

Figure 4 Schematic of Dynamic Latch Comparator

During reset mode the input voltage difference is established at node A_1 and A_2. The regeneration happens during a small time when φ1 is rising and φ2 is falling. At the end of regeneration process the SR latch is driven to the digital output levels. The power consumption of the comparator is 33μW at a frequency of 225MHz.

This design was implemented at 180 nm CMOS technology operating at a ±1.8 V power supply with 8-bit of resolution and input range of 1.8 V. And transistor widths are calculated as per the comparator requirement [2].

$W_{12} = 4u$m, $W_1 = 6u$m,
$W_8 = 4u$m, W10 = 10um,
$W_6 = 30u$m

These widths are calculated by using following formula

$$\tau_{reg} = \frac{(\alpha W_4 + C_P)}{\sqrt{\frac{2 I_4 W_4}{L_4 K_{pm}}}} \qquad (2)$$

Considering $\alpha W_4 = C_p$

3.1.Bit binary synchronous counter

Counters are among the most basic of designs in digital systems. Along with being simple to make, counters, in general, are archetypical components of most digital systems as they are used to store (and sometimes display) the number of times a particular event has occurred. The different number of implementations of a 5-bit counter is vast. With options such as synchronous vs asynchronous, why flip-flops to use, and the style of counting (binary, gray-code, etc).

The counter described here is designed to be a synchronous up-counter as shown in Figure 5. This means that the whole design is controlled by one single clock and that the counter will only count from 0 to F and start back over. This counter is realized using D flip-flops [6].

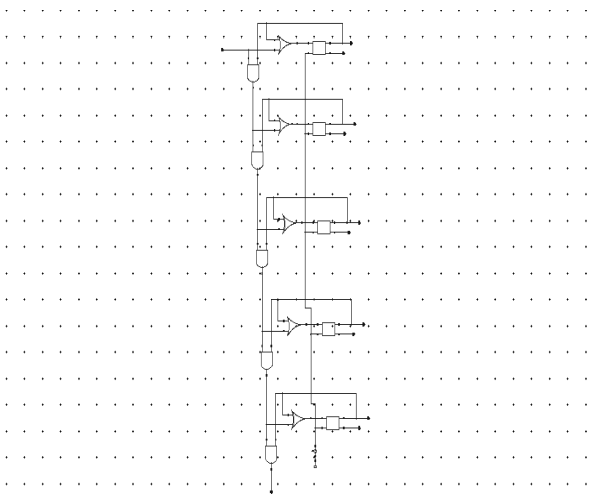

Figure 5 Schematic of 5-bit counter

The D flip-flop was chosen because of its simplicity over the design of JK flip-flop; it only takes one input instead of two, and requires less interconnect which should lead to less delay. Also, the synchronous up-counter nature of the design was chosen because simple design. This counter is counting from 0 to 1.8 volts, with a precision of 0.59375V.

3.1 5-Bit 2:1 Mux-Latch

With current topologies, dynamic latches are widely used in the high performance VLSI circuits, mainly due to lower cost and higher operation speed than static latches. Figure 6 depicts the preferred dynamic latch circuit. This latch circuit either transfers the input logic level to the output (during clock signal is kept at logic "1") or keeps the last output logic level (during clock signal is kept at logic "0") all depends on the controlling clock signal.

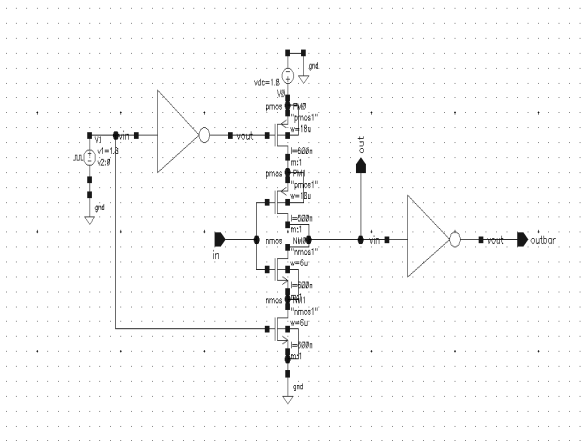

Figure 6 Schematic of Dynamic latch

In other words, clock "0" means conversion phase, and clock "1" means sampling phase. This control between digital and analog parts of ADC is obtained. In fact, it is not possible to convert an analog input level to its digital value immediately. A very small time period is essential for the digital part to complete its job. Therefore, a dynamic latch circuit use to make inevitable for ADC

design. This time is called as “conversion time” in general and it is shortest in I-F ADCs, but very long for serial type of ADCs.

The output of the latch is given as input to 2:1 mux and is also used as select line for the mux of next block as shown in Figure 7, for 5-bit resolution.

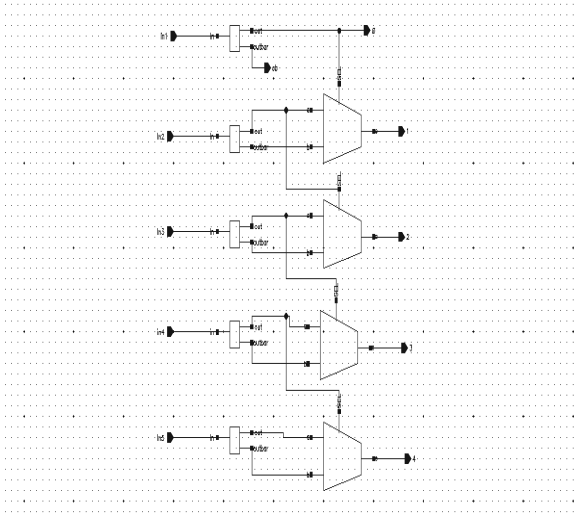

Figure 7. Circuit diagram of 2:1 mux type latch

3. POWER REDUCTION

While designing any CMOS circuit power is a very important issue and in ADC we always required low power. This power can be reduced by using low power techniques such as decoupling capacitor, variable frequency, Clock gating, scaling down voltage etc. Clock gating technique is one of these power reduction techniques adopted in this design is shown in Figure 8

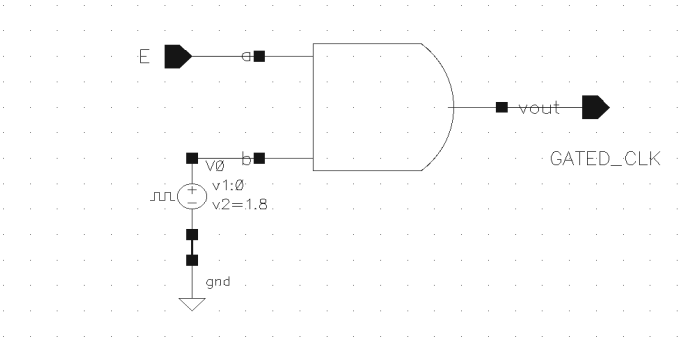

Figure 8 Circuit of Clock gating without latch

4. RESULTS

Designing, schematics, simulation and comparison of various performance parameters were done for two different ADC’s. Simulations were carried out using Cadence Tools. The present work,

technology taken is 12.3 nW with sampling frequency of 225MHz and a power supply of 1.8V. A 5-bit data is achieved with a power of 12.3nW, as shown in Table.1

Table.1 Design Specifications

Parameters	**Value**
Technology	180nm
Sample frequency	225 MHz
Power Supply	1.8 V
Stop time	200 ns
Resolution	5 bits
Power	12.3*n*W
Reference Voltage	1.8 V

The transient response of the I-F ADC is shown in Fig.9 output waveform is collected from the 5-bit latch, which is collected in parallel form. This 5 bit data has sampling rate of 225MHz.

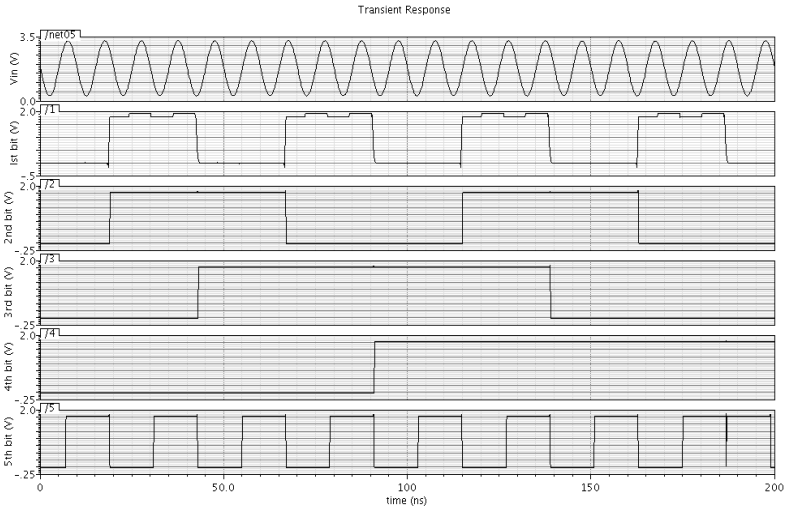

Figure 9 Transient response of I-F ADC

The waveform is taken with a stop time of 100ns.The first bit is MSB and last one in LSB of ADC's output. The designed ADC results are compared with the current I-F ADC and the flash ADC [7]. Table2 shows the comparison between these two ADC's. Reference ADC is done at 0.6 um, so firstly design with same parameters, then with 180 nm technology and got a improved power of 1.1μW at a sampling frequency of 225 MHz with a improved resolution of 5 bit from 4.25 and by using clock gating technique get the power of 12.3nW.

Table1. Comparison between flash and current-frequency ADC's

	PREVIOUS WORK		**PRESENT WORK**	
Parameters	**Flash ADC**	**I-F ADC**	**I-F ADC**	**I-F ADC**
Technology	180nm	0.6 μm	0.6 μm	180nm
Resolution(bits)	3	4.25	5	5
Power supply	1.8 V	1.2 V	1.8V	1.8V
Power(W)	0.85m	1.3μ	1.1μ	12.3n
Sampling Freq.(MHz)	150	225	225	225

5. CONCLUSION

This paper presented low power 5-bit current- frequency ADC design at 180 nm technology. This ADC is designed for implantable blood glucose monitoring. With improvement in the power consumption of 180nW at 225MHz sampling frequency and power supply of 1.8 V.

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