LOW VOLTAGE, HIGH SPEED AND HIGH TEMPERATURE OF 1T-1C DRAM IN CMOS 3C-SiC 250nm TECHNOLOGY

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ABSTRACT

The digital electronics field is becoming increasingly present in very hostile environments where the temperature is very high. In these environments, the wide bandgap materials such as silicon carbide (SiC) to replace silicon (Si). In this paper, we have studied the one-transistor one-capacitor Dynamic Random Access memory cell (1T-1C DRAM) in CMOSiC-3C 250nm technology. To perform this work we have used PSpice level 3 to study the DC characteristics of MOSiC-3C transistors 250nm technology, and then depending on these characteristics, we studied the most important operations read/write and refresh related to the 1T-1C DRAM cell. This is study has given very excellent results, where we found that our DRAM cell operate under a low supply voltage 2V, wide temperature range from 27°C to 300°C and characterized by high speed operations.

KEYWORDS

3C-SiC, PSpice level 3, 250nm technology, CMOS, 1T-1C DRAM.

1. INTRODUCTION

Silicon carbide (SiC), a wide bandgap (WBG) semiconductor material, considered as one of the basic materials for making transistors that are working with high power, high frequency and high temperature due to its better physical properties than silicon (Si). It has a high breakdown field, a high saturation velocity of electrons and a high thermal conductivity [1], and has the potential to overcome the limitations imposed by power devices made of Si base material [2-3-4]. However, recent studies have shown that the Metal Oxide Semiconductor (MOS) transistors in silicon carbide submicron technology work well in low voltage, low power, high frequency and high temperature [5-6].

Dynamic Random Access Memory (DRAM) is a prominent product of semiconductor industry [7] in which this cell is found in virtually every computer in use today, this is due to their importance in the field of digital electronics. Among the proposed designs for the DRAM cell, the concept of One-Transistor, One-Capacitor DRAM (1T-1C DRAM) appeared out more than 20 years ago [8] in which these devices are known as single-transistor capacitorless 1T-DRAM memories in the case of integration [9-10]. Silicon technology has been widely used in the manufacturing of these cells, because of the up notable achievements of this technology of memory-related technology over the past two decades.

In this respect, we will propose other semiconductors to manufacture the DRAM cells as an alternative to silicon technology.

In this work, we propose for the first time a new 1T-1C DRAM cell in CMOSiC-3C 250nm technology. The first part of our work consists in presenting the use of PSpice level 3 as a model for our MOSiC-3C transistors. Based on the equations of this model [11-12], we calculate NMOSiC-3C and PMOSiC-3C transistors, then simulate output $I_D=f(V_{DS})$ and transfer $I_D=f(V_{GS})$ characteristics for these transistors, and consequently, we integrate our transistors in the inverter circuit to verify the operation of these transistors in switching mode. We will use our transistors to study 1T-DRAM cell in the second part, through analyzing this cell characteristics Read/Write and Refresh operations, and discuss key factors affecting device characteristics. Finally, we also show the scalability of the proposed cell in this technology for operation in other conditions. Our work is carried for 250 nm channel length; 3V and 2V supply voltage for MOSiC-3C transistors and 1T-1C DRAM respectively at temperatures between 27°C and 300°C.

2. DESCRIPTION OF THE TRANSISTOR AND 1T-1C DRAM CELL

To achieve the objectives of this work, we use the parameters of N and PMOS transistors which show the different dimensions and doping technologies, in the following table.

Table I. Physical parameters of 3C-SiC N and PMOS transistors.

Designation	**Symbol**	**NMOS**	**PMOS**	**Unit**
Channel length	L	250	250	nm
Channel width	W	400	4000	nm
Lateral Diffusion Length	L_D	5	5	nm
Drain and Source Length	L_{diff}	1200	1200	nm
Drain and source depth	X_j	300	300	nm
Oxide thickness	T_{OX}	5.7	5.7	nm
Substrate doping	N_{SUB}	9.10^{17}	10^{15}	cm^{-3}
Drain, Source and Gate doping	$N_D=N_S=N_G$	10^{20}	10^{20}	cm^{-3}

As for our DRAM cell, we use the equivalent circuit of the 1T-1C DRAM cell shown in the Figure 1.

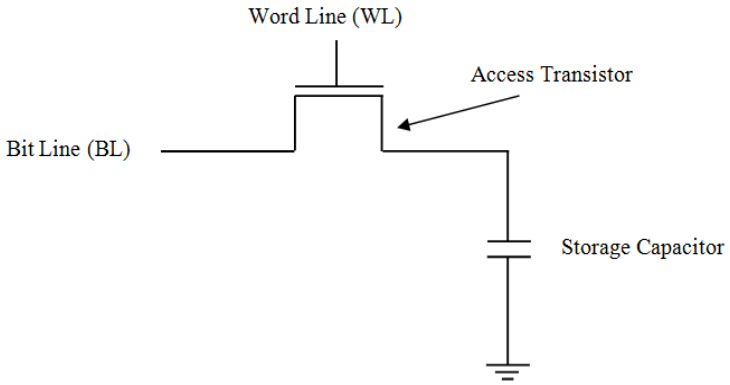

Figure 1: Equivalent circuit of the 1T-1C DRAM cell [13].

3. RESULTS AND DISCUSSION

3.1 DC characteristics of MOSiC-3C transistors:

3.1.1 Output characteristics $I_D=f(V_{DS})$:

Fig. 2 shows the evolution of the drain current as a function of the drain voltage of the NMOSiC-3C and PMOSiC-3C transistors at two temperature values 27°C and 300°C, at the variation of the gate voltage between 0V and 3V.

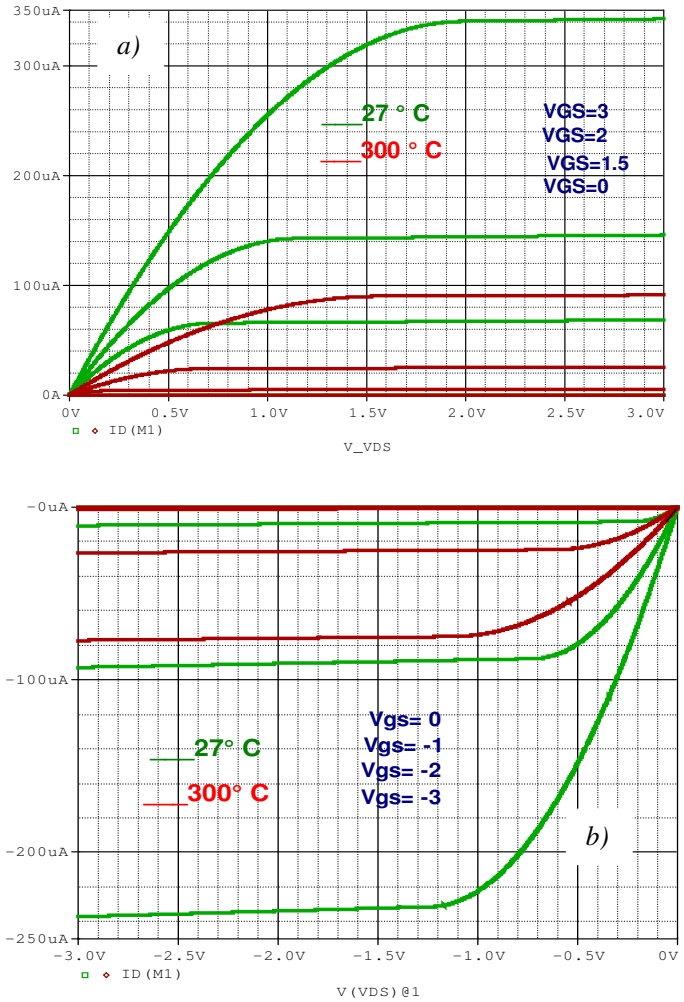

Figure 2: Output characteristics $I_D=f(V_{DS})$ of MOSiC-3C transistor, a) NMOS transistor, b) PMOS transistor.

Fig 2 shows that our transistors are working properly because the input characteristics contain the linear (Ohmic) and saturation parts. The drain current of the MOS transistors in 3C-SiC technology is decreased as the temperature increases as shown in figure 3. These results show that MOSiC-3C transistors in 250nm technology work well in low voltage, in less than 3V, low power and high temperature of about 300°C. This is consistent with what is stated in the literature [5].

3.1.2 Transfer characteristic $I_D=f(V_{GS})$

Fig 3 shows the transfer characteristic $I_D=f(V_{GS})$ of NMOSiC-3C and PMOSiC-3C transistors at voltage V_{DS} = 3V and in a temperature range of 27°C to 300°C.

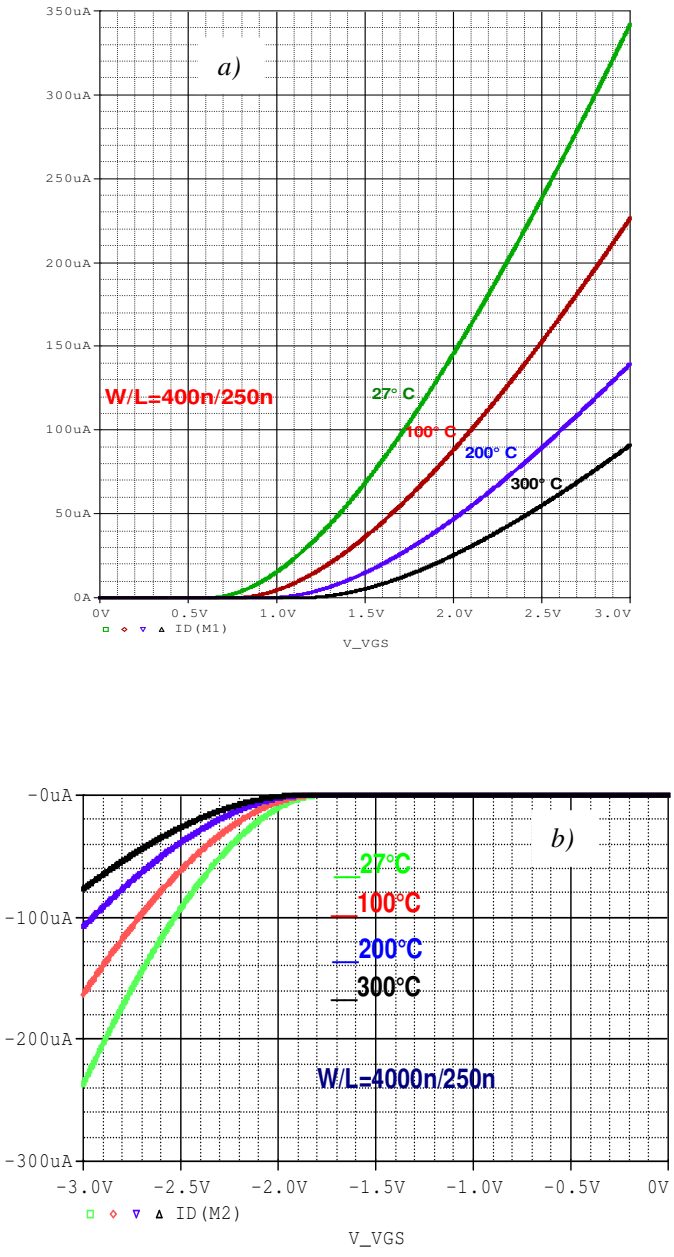

Figure 3: Transfer characteristic $I_D=f(V_{GS})$ of MOSiC-3C transistors, a) NMOS transistor, b) PMOS transistor.

I_D = f (V_{GS}) is a very important characteristic of a MOS transistor that is exploited to find the threshold voltage. The influence of temperature on this characteristic is represented by Fig 3. This figure shows that the threshold voltage is directly proportional with the temperature variation.

This shows that the transconductance of our transistors are decreased as a function of temperature.

The simulation results show that our transistors are characterized by better electrical characteristics this allows it to manufacture analogue and digital electronic systems.

3.2 Static CMOSiC-3C inverter

Fig 4 shows the circuit diagram of static CMOS inverter in 3C-SiC technology. The inverter is truly the nucleus of all digital designs that consist of the NMOS and PMOS transistors which in turn are processed and connected [14], as shown in this figure.

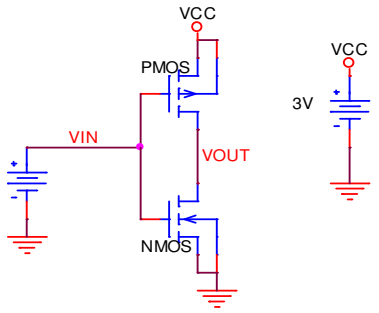

Figure 4: Circuit diagram of static CMOSiS-3C inverter.

The simulation results of this inverter are given the Fig 5. This figure shows the voltage transfer characteristics (VTC) of our inverter at four different temperatures with a voltage supply of 3V.

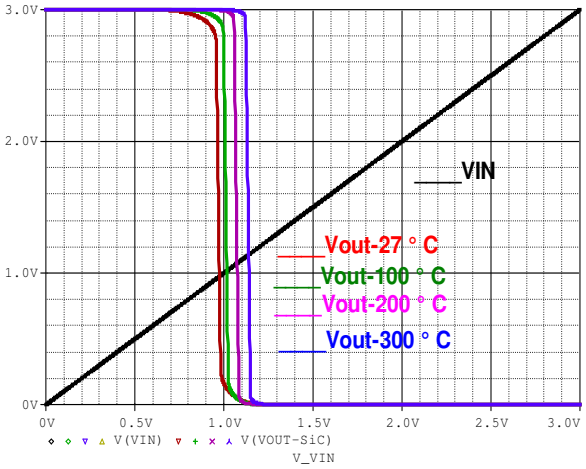

Figure 5: Voltage transfer characteristics (VTC) of static CMOSiC-3C inverter

Voltage transfer characteristic (VTC) gives the response of the inverter circuit, V_{OUT} as a function of the V_{IN}. The transition from the ON to the OFF state is done when the V_{IN} value close to $V_{CC}/2$. Lack of precise symmetry in our transistors parameters is responsible for this displacement. Results show that our inverter in CMOSiC-3C technology is characterized by high operating capacity in a wide temperature range. Voltage transfer characteristics (VTC) of the static CMOSiC-3C inverter showed that our transistors functioned well in switching mode.

3.3 1T-1C DRAM in 3C-SiC technology

3.3.1 Read/Write operation

When an electric charge is stored in a capacitor, it corresponds to a logical state (logical 1), and the absence of charge in capacitor corresponding to the other logical state (logical 0). This is adopted principle in the design of the dynamic memory cell 1T-1C DRAM. Fig 6 shows the simulation scheme of the Read/Write operation of our DRAM cell in CMOSiC-3C technology at supply voltage 2V.

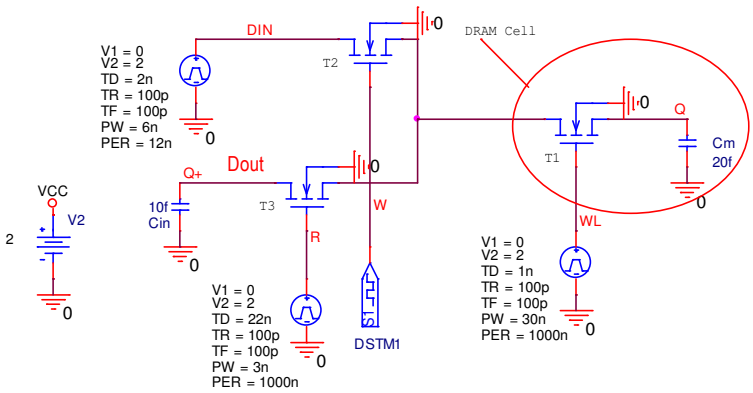

Figure 6: Simulation scheme of the Read/Write operation of DRAM cell in CMOSiC-3C.

The results of this DRAM cell are given the Fig 7, which shows the chronogram of the Read/Write operation of our DRAM cell in CMOSiC-3C technology at room temperature and 300°C.

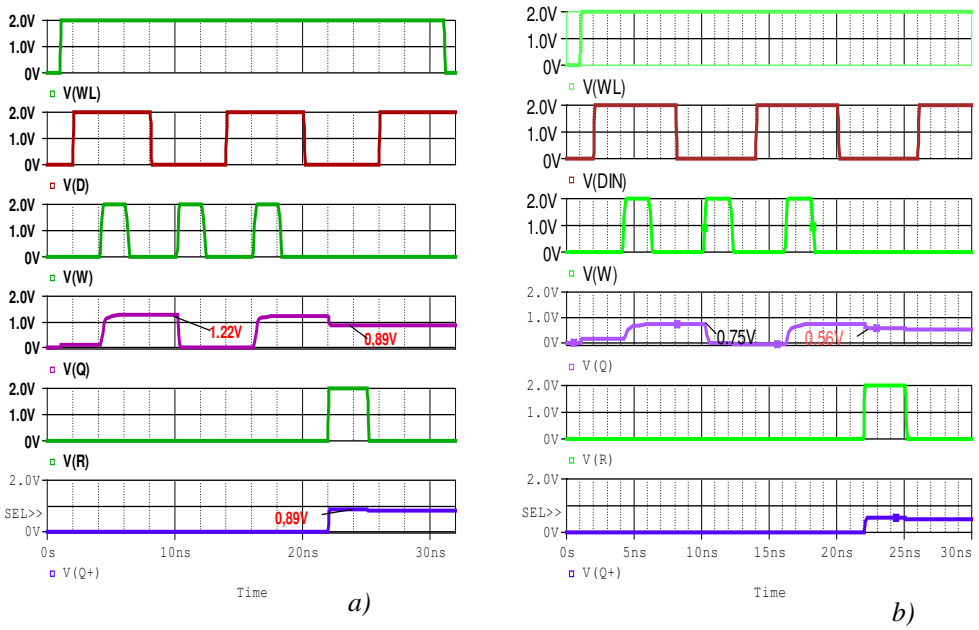

Figure 7: Chronogram of the Read/Write operation of 1T-DRAM cell in CMOSiC-3C, a) at 27°C, b) at 300°C.

The functioning of our DRAM cell according to this chronogram is shown as follows:

- At t = 1ns: WL = 1, the memory point is selected.
- At t = 4ns: D = 1 and W = 1, there is a write order of a logical 1. The capacitor charges through T1 and T2 to the high level (1).
- At t = 10ns: D = 0 and W = 1, there is an order to write a logical 0. The capacitor discharges through T1 and T2 to the low level (0V).
- At t = 22ns: Q = 1 and R = 1, there is a reading order of a logical 1. Capacitor C partially discharges through T1 and T3 (C_{in} load).

These results show that 1T-1C DRAM cell in CMOSiC-3C is working properly, although the temperature is high 300°C, and show that this cell is characterized by higher speed Read/Write operation because the cycle time 22ns. This study shows that 1T-1C DRAM cell in CMOSiC-3C 250nm technology has good features compared to those in presented in the literature Table II.

Table II. Properties of 1T-1C DRAM in CMOSiC-3C 250nm technology compared to different other DRAM cells.

Materials	**Si**	**Si**	**Si**	**Si**	**3C-SiC**
Technology	28nm	150nm	45nm	250nm	250nm
Structure DRAM	FDOSI -1T	FDOSI -1T	1T-1C	1T-1C	1T-1C
Supply voltage	1.5V	1.8V	1V	3.3V	2V
Cycle time	320ns	40ns	-	20ns	22 ns
Temperature range (°C)	25 - 85	25 - 85	25	25	27 - 300
References	[7]	[15]	[16]	[17]	This work

3.3.2 Refresh of 1T-1C DRAM

DRAM cells rely on periodic refresh operations to maintain data integrity. Refresh operations contend with read operations, which increases read latency and reduces system performance [18]. Fig 8 shows our design of a refresh circuit of 1T-1C DRAM in CMOSiC-3C technology.

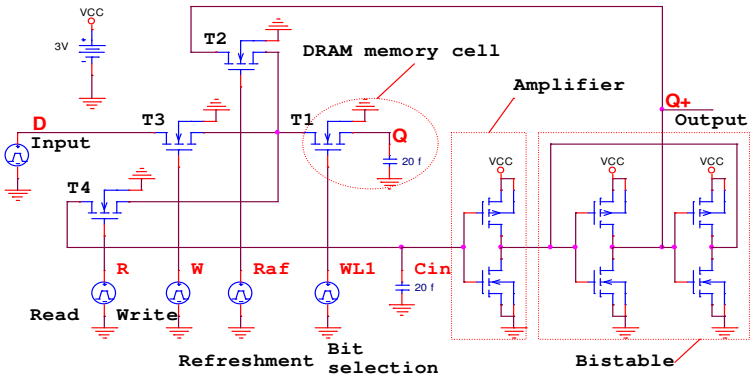

Figure 8: Simulation schema of a refresh circuit of DRAM in CMOSiC-3C.

Fig 9 shows timing diagrams of the refresh operation of a DRAM cell in CMOSiC-3C technology for two temperature values 27°C and 300°C at supply voltage 3V.

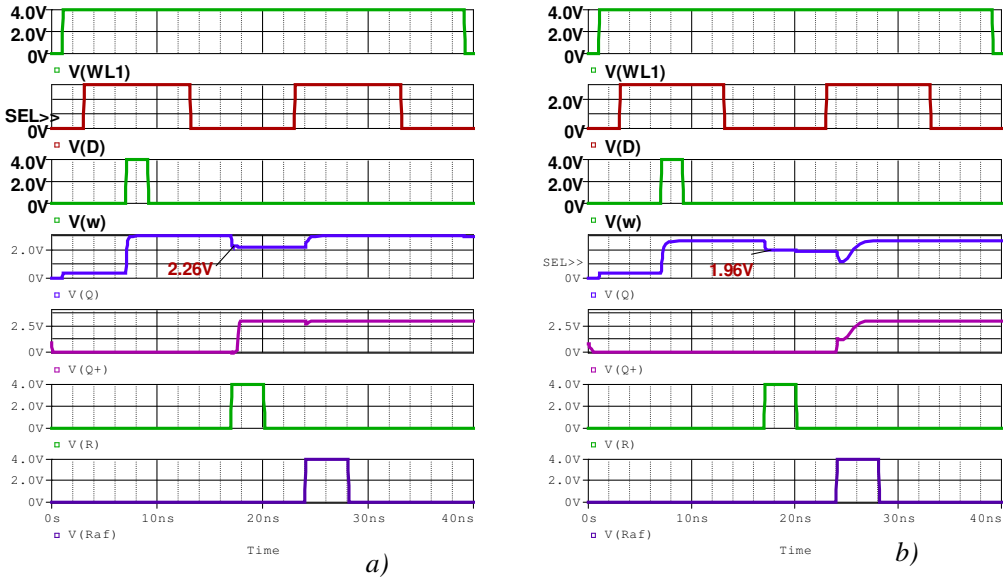

Figure 9: Timing diagrams of the refresh operation of a DRAM cell in 3C-SiC technology, a) at 27 ° C, b) at 300°C.

The configuration of the amplifier (CMOS inverter) followed by a bistable allows to keep the state of Q during reading in order to rewrite it again.

- At t = 1 ns: WL1 = 1, the memory cell is selected,
- At t = 7ns: D= 1 and W= 1, there is an order to write a logical 1. The capacitor C is charged through T3 and T1 to V_{CC} (VQ=3V), and it remains charged.
- At t = 17ns: R = 1, there is a reading order. The capacitor is partially discharged to 2.26V through T4 and T1, at the same time, the output of the amplifier is switched to V_{CC} and stays at this state.
- At t = 24ns: Raf = 1, there is a refresh order. The capacitor C is recharged by the bistable through T2 and T1 until V_{CC}=3V.

The design shows that 1T-1C DRAM cell in CMOSiC-3C 250nm technology has a better refresh operation, so that the information is maintained and not lost despite the high temperature.

4. CONCLUSION

Our N and PMOS transistors are calculated for 3C-SiC 250nm technology, then simulated by the PSpice level 3 model. This simulation shows that our MOSiC-3C transistors operate correctly in a temperature range of 27°C to 300°C for 3V supply voltage. According to the inverter simulation, we have shown that our transistors work properly in switching mode. As a result, we used these transistors to study the functioning of the 1T-1C DRAM cell in CMOSi-3C 250nm technology. The timing diagrams obtained showed the good functioning of our 1T-1C DRAM cell in terms of

low power, high speed and high temperature. This is what is demanded by embedded electronic systems, and this cell has the advantage of using in hostile and severe environments.

REFERENCES

[1] Laurence Latu-Romain, Maelig Ollivier. (2015) “Silicon Carbide One-dimensional Nanostructures” ISTE Ltd -WILEY-Library of Congress Control Number: 2014955862.

[2] A. Fayyaz and A. Castellazzi. (2015)"High temperature pulsed-gate robustness testing of SiC power MOSFETs" Microelectronics Reliability 55. 1724–1728.

[3] A. Ibrahim, J.P. Ousten, R. Lallemand and Z. Khatir. (2016)"Power cycling issues and challenges of SiC MOSFET power modules in high temperature conditions" Microelectronics Reliability 58. 204–210.

[4] A. Castellazzi , A. Fayyaz, G. Romanob, L. Yanga, M. Ricciob and A. Irace. (2016)" SiC power MOSFETs performance, robustness and technology maturity" Microelectronics Reliability 58. 164–176.

[5] Mourab hebali, Djilali Berbara, Mohammed Benzohra, Djalali Chahali, Abdelkader Saïdane and Abdlekader Baghdad Bey. (2017) ‘MOSiC (3C, 4H and 6H) Transistors 130nm by BSIM3v3 Model in Low Voltage and Low Power’ Journal of Engineering Science and Technology Review 10 (5) 195 – 198.

[6] Jędrzej Stęszewski, Andrzej Jakubowski, and Michael L. (2007) “Copmarison of 4H-SiC and 6H-SiC MOSFET I-V characteristics simulated with Silvaco Atlas and Crosslight Apsys” Journal of Telecommunications & Information Technology .2007 (3).. Pp 93-95.

[7] H. El Dirani , K.H. Lee , M.S. Parihar , J. Lacord, S.Martinie , J-Ch. Barbe , X.Mescot , P. Fonteneau , J.-E. Broquin , G. Ghibaudo , Ph. Galy, F. Gamiz , Y. Taur , Y.-T. Kim, S. Cristoloveanu, M. Bawedin. (2017) "Ultra-low power 1T-DRAM in FDSOI technology" Microelectronic Engineering 178. 245–249.

[8] Wann, H.J., Hu, C (1993) “A capacitorless DRAM cell on SOI substrate. In: Electron Devices Meeting IEDM’93” Technical Digest International, pp. 635–638.

[9] S. Okhonin, M. Nagoga, J.M. Sallese, P. Fazan. (2002) “A capacitor-less 1T-DRAM cell”, IEEE Electron Device Lett. 23 (2) 85-87.

[10] T. Tanaka, E. Yoshida, T. Miyashita, (2004)” Scalability study on a capacitorless 1T-DRAM: from single-gate PD-SO1 to double-gate FinDRAM”, IEEE International Electron Devices Meeting (IEDM), pp. 919–922.

[11] Akio Kitagawa. (2013) “Modeling of MOSFET for analog design” Kanazawa University Microelectronics Research Lab.

[12] Andrei Vladimirescu. (1999) “MOSFET Modeling in SPICE” UC Berkeley EE241.

[13] Takashi Ohsawa,Takeshi Hamamoto. (2012)" Floating Body Cell: A Novel Capacitor-Less DRAM Cell " 1st Edition, Taylor & Francis Group.

[14] R, Jacob Baker. (2010) “CMOS Circuit Design Layout and Simulation” 3rd Edition IEEE.

[15] K.R.A. Sasaki, T. Nicoletti, L.M. Almeida, S.D. dos Santos, A. Nissimoff, M. Aoulaiche, E. Simoen, C. Claeys, J.A. Martino (2014)" Improved retention times in UTBOX nMOSFETs for 1T-DRAM applications" Solid-State Electronics 97 pp.30-37.

[16] Sherif M.Sharroush(2016) " Performance optimization of 1T-1CDRAMs: A quantitative study" Microelectronics Journal 52pp.147–164.

[17] J. A. Mandelman, R. H. Dennard, G. B. Bronner, J. K. DeBrosse, R. Divakaruni, Y. Li and C. J. Radens (2002)"Challenges and future directions for the scaling of dynamic random-access memory (DRAM)" IBM J. RES. & DEV. VOL. 46 NO. 2/3 MARCH/MAY.

[18] Prashant Nair, Chia-Chen Chou and Moinuddin K. Qureshi. (2013)"A Case for Refresh Pausing in DRAM Memory Systems" IEEE 19th International Symposium on High Performance Computer Architecture (HPCA).